Approved By Fred J. Potter Date 5-9-2000
(Engineering)

Approved By Jim Zeoli Date 6-6-2000
(Quality Assurance)

Approved By M. Aldrich Date 5/10/2000
(Supplier Quality Assurance)

REVISION STATUS:

Rev.	Approved Eng.	QA	PR.	Rev.	Approved Eng.	QA	PR.
A	JFP	MF	-				
B	FJP	MF	-				
C	FJP	JZ	-				
D	GRL	JZ	-				
E	GRL	JZ	-				
F	GRL	JZ	-				
G	GRL	RM	-				
H	GRL	SA3	-				
J	GRL	SA3	-				
K	GRL	SA3	BKP				

AMETEK®
AEROSPACE
HARLEYSVILLE, PA 19438
CAGE 61349

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REVISIONS

REV.	DATE	DESCRIPTION
A	2/19/97	Initial release.
B	9/9/97	Para. 1.0, deleted word "procurement". Para. 2.1, clarified the order of precedence. Para. 3.0, Added reference to IPC specifications. Para. 3.2, added phrase "no tighter than" to thickness tolerance. Para. 3.8, added grade B to gold plating criteria, removed prohibition against gold under soldermask. Para. 3.9 & 3.11, replaced "per AMETEK spec MS-1004" with "per IPC-6012". Para. 3.13, reorganized into para. 3.13.1, 3.13.2 and 3.13.3; added test and inspection criteria, updated ref to ANSI/IPC-600. Para. 3.14, clarified packaging requirements.
C	2/5/00	First Page, added Supplier Quality Assurance approval. Para. 2.0, added following documents: IPC-2222, IPC-4101, IPC-6013, IPC-MF-150, IPC-FC-231, IPC-FC-232, IPC-FC-241, IPC-AI-642, IPC-ET-652, IPC-SM-840, J-STD-003, J-STD-006, MIL-S-13949, MIL-PRF-55110, MIL-P-50884, ASTM B488-95 Completely rewritten.
D	11/22/04	Through out this document, in 16 places, changed "procurement drawing" to "PCB document". Para. 1.0, removed "The AMETEK test philosophy is to test printed circuit assemblies for assembly workmanship and component defects. It is not designed to test for bare board defects; therefore, it is imperative that we receive good bare boards from the vendor." Para. 3.1, added "All AMETEK rigid printed circuit boards shall be constructed with FR-4 material in accordance with IPC-4101/21 or /24, unless otherwise specified."
E	02/18/05	Completely rewritten with recommendations from PWB consultant. Title Block: Changed "AEROSPACE FABRICATION SPECIFICATION FOR PRINTED CIRCUIT BOARDS" to "AEROSPACE FABRICATION SPECIFICATION FOR RIGID AND FLEXIBLE PRINTED WIRING BOARDS". Added Para. 3.4.4, "VIAS IN SMT PADS".

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REVISIONS

REV.	DATE	DESCRIPTION
F	04/22/05	Incorporated feedback from vendors. Para 3.1, added the option to use /21 material. Para 3.12.3, added paragraph on test results. Para 3.13, added specs for Certificate of Compliance. Para 3.14, added desiccant bag for shipping.
G	11/02/05	Para 3.3, Changed "Also the starting copper foil for external layers shall be 1 oz plus copper plating." To: "Unless otherwise specified on the drawing, the finished external copper layer thickness shall be equivalent to 1 oz (0.0012") minimum." Added the following sentence to the end of the first paragraph: "Unless otherwise specified on the drawing, the dielectric spacing between copper layers shall be 0.0035" minimum (reference see Figure 3-14 of IPC 6012B)." Para 3.13, Changed "Cross-sections and solder samples shall be submitted with each shipment." To: "Unless otherwise specified in writing by Ametek's Quality Engineer, all potted microsections representing the acceptable lot shall be shipped with the boards."
H	10/11/06	Para 3.12.3, Added Inspection criteria to include inspecting 1 board per order 100% for hole sizes and outlying dimensions if applicable. Para 3.13, Added purchasing requirement to make sure paper work matches before PWB's are built. Added first article inspection. Added digital picture requirements along with attached digital samples. Eliminated solder stressed circuit board. Para 3.14, Added packaging requirement up to 10 boards and criteria for lead free boards. Para 4.0, Added Engineering sheet.
J	7/11/12	Para 3.13, Added: "Cross section data shall be submitted with each shipment. The data must include part number, supplier, and date code." Added: "Test data (EOL yield) by serial number must be supplied with each shipment, cross section parts, and all build information to be retained for 3 years."

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K	3/19/13	Para 3.11, Changed "shall contain supplier trademark, date code, and serial numbers". To: "shall contain supplier trademark, date code, and if possible or if requested, serial numbers". Para 3.13, Changed "Supplier shall issue a C of C (Certificate of Compliance)A first Article inspection (only with first-shipment or a Rev change that effects the outline configuration or dimension)". To: "Supplier shall issue a C of C (Certificate of Compliance) with every shipment. A First Article inspection must be issued with every first-shipment or a shipment that includes a rev change that effects the outline configuration or dimension". Para 3.13, Changed "Unless otherwise specified in writing by Ametek's Quality Engineer, all solder stressed samples must be stored at the supplier and only Digital pictures of a large and small hole(solder stressed at 280C) for each panel shall be sent with the test report showing the copper thickness measurement (See samples). Each must be identified to the item's part number, supplier, date code and serial number". To: "Unless otherwise specified in writing by Ametek's Quality Engineer, all solder stressed samples must be stored at the supplier for 3 years. Digital pictures of a large and small hole(solder stressed at 280C) for each panel shall be sent with the test report showing the copper thickness measurement if requested. Each image if supplied must be identified to the item's part number, supplier, date code and serial number if applicable". Para 3.4.1, Changed "The number and finished (plated) size of all holes is specified on the PWB drawing." To: "The number and finished (plated) size of all holes is specified on either the PWB drawing or the Drill Tape file. Finished hole tolerance is +/- 0.003 unless otherwise specified." Para 3.5, Changed "Photoimageable per IPC-SM-840, class H." To: "Photoimageable per IPC-SM-840, class H. Color Green unless otherwise specified."

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1.0 SCOPE

This specification performs two functions:

a) It provides a standard set of fabrication notes for printed wiring boards and flexible printed circuits, and serves to update obsolete drawing notes and references to allow suppliers to utilize best commercial practices where possible.

b) It defines the criteria for selecting Aerospace approved sources for printed wiring boards for the Aerospace Products Group.

The AMETEK Purchasing Department must only obtain Bare Printed Wiring Boards (PWBs) from the sources able to meet the criteria listed in this document. All new vendors must be certified according to the procedures developed for vendor certification.

2.0 REFERENCE DOCUMENTS

IPC-2222	Sectional Design Standard on Printed Board Design
IPC-4101	Specification for Base Materials for Rigid and Multilayer Printed Boards
IPC-6011	IPC Specification, Generic Performance Specification for Printed Boards.
IPC-6012	Qualification and Performance Specification for Rigid Printed Boards
IPC-6013	Qualification and Performance Specification for Flexible Printed Boards
IPC-MF-150	Copper Foil for Printed Wiring Applications
IPC-FC-231	Flexible Base Dielectrics for use in Flexible Printed Wiring
IPC-FC-232	Adhesive coated Dielectric films for Use as Cover Sheets for Flexible Printed Wiring and Flexible Adhesive Bonding Films
IPC-FC-241	Flexible Metal-Clad Dielectrics for Use in Fabrication of Flexible Printed Wiring
IPC-D-325	Documentation Requirements for Wiring

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IPC-A-600	Acceptability of Printed Boards
IPC-AI-642	User's Guidelines for Automated Inspection if Artwork, Innerlayers, and Unpopulated PWBs
IPC-9252	Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards
IPC-SM-840	Qualification and Performance of Permanent Solder Mask
J-STD-003	Solderability Tests for Printed Boards
J-STD-006	Requirements for Electronics Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications
MIL-S-13949	Sheet, Printed Wiring Board, General (MIL-P-13949) Specification For (Cancelled)
MIL-PRF-55110	Printed Wiring Board, Rigid, General (MIL-P-55110) Specification For (Inactive for New Design)
MIL-PRF-31032	Performance Specification Printed Circuit Board/Printed Wiring Board, General Specification for
MIL-P-50884	Printed Wiring Board, Flexible and Rigid-Flex, General Specification For
ASTM B488-95	Standard Specification for Electrodeposited Coatings of Gold for Engineering Uses
AS-9102	AEROSPACE FIRST ARTICLE INSPECTION REQUIREMENT

2.1 UNIQUE TERMINOLOGY AND DEFINITIONS

The following terms are defined for use within this document.

PWB Fabrication Spec.	This document
PWB Drawing	Contains vital information on PWB details, dimensions and construction. Formerly known as Drill drawing, Procurement drawing, Fabrication drawing, PCB drawing and Fabrication document.

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2.2 ORDER OF PRECEDENCE

This document shall serve to augment and update the PWB drawing notes for all AMETEK Aerospace (Harleysville) Printed Wiring Boards. In the event of a conflict between this document and the PWB drawing, this document takes precedence unless otherwise noted. Notes or instructions placed on the purchase order have precedence over this document.

3.0 PRINTED WIRING BOARD FABRICATION SPECIFICATIONS

All AMETEK rigid printed boards and flex circuitry shall be fabricated in accordance with IPC-6011 and IPC-6012, as applicable, to the latest revision level. All panels shall contain conformance coupons in accordance with IPC-2221 (latest rev. level) and tested in accordance with IPC-6012 or IPC-6013 as applicable. Note: a land representing each layer shall be exhibited in each PTH of the coupon.

All rigid printed boards containing 4 layers or less shall meet the requirements of IPC-6011 and IPC-6012, Class 2 unless otherwise specified on the PWB drawing or purchase order.

All rigid printed boards containing more than 4 layers shall meet the requirements of IPC-6011 and IPC-6012, Class 3 unless otherwise specified on the PWB drawing or purchase order.

All flexible circuits containing 4 layers or less shall meet the requirements of IPC-6011 and IPC-6013, Class 2 unless otherwise specified on the PWB drawing or purchase order.

All flexible circuits containing more than 4 layers shall meet the requirements of IPC-6011 and IPC-6013, Class 3 unless otherwise specified on the PWB drawing or purchase order.

Flexible circuits must be able to withstand low cycle flexing for service and testing. Rigid/Flex boards are referred to as “flexible circuits” in this document.

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Acceptance testing shall be based upon the requirements as specified in IPC-6012 or IPC-6013, latest rev levels. Inspection criteria, as a supplement, shall be per IPC-600 latest rev level. If a conflict exists between IPC-6012 or IPC-6013 and IPC-600, the fabrication specs (IPC-6012 & IPC-6013) shall take precedence. The lot size definition as specified in IPC-6011 paragraph 4.3.2.1 is not to be used. The following lot definition is to be used for AMETEK procurement: Production boards may be combined from the same or different lots to form an inspection lot providing it consists of one part number fabricated from the same material, using the same processing procedures and construction, produced under the same conditions and offered for inspection at one time.
Note: combining printed boards/panels with other part numbers and other customers is not considered a part of a lot. Each part number/lot shall meet the sampling plan and/or 100%inspection or test as specified in IPC-6012 and IPC-6013 (latest rev levels) as applicable. Other exceptions to IPC-6011, IPC-6012 and IPC-6013 are noted below.

Note: The sampling plan as specified in IPC-6012 has acceptance of C=0 (zero defect). This means that if a defect is found, the whole lot shall be screened 100% for that defect. If any obvious other defect(s) is found it shall not be ignored. Those defects shall be removed from the lot also.

3.0.1 MIL-PRF-31032 or MIL-P-50884 requirements only apply if specifically referenced as a QC Code on the Purchase Order. (Reference AMETEK Supplementary Terms and Conditions.)

3.1 MATERIAL

All AMETEK Class 2 (four layers or less) rigid printed wiring boards shall be constructed with FR4 material in accordance with IPC-4101/21 or /24, unless otherwise specified on the purchase order. All AMETEK Class 3 (containing over 4 layers) rigid printed wiring boards shall be constructed with FR4 material in accordance with IPC-4101/24 (min Tg 170 deg C), unless otherwise specified on the purchase order.

Where "G-10" or FR-4, or MIL-S-13949/4 or /12 material is called out on the PWB drawing, laminate and prepreg material shall be in accordance with IPC-4101/21 or /24 as applicable in above paragraph.

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Where polyimide, GI, or MIL-S-13949/10 or /13 materials are called out on the PWB drawing, laminate and prepreg materials shall be in accordance with IPC-4101/40 or /42.

Surface quality shall be B. Thickness tolerances shall be sufficient to meet total stackup thickness tolerance indicated on the PWB drawing. Laminates with lower resin contents should be utilized where options exist for the same thickness material to minimize z-axis expansion coefficients, unless certain processing requires the use of high resin content material, e.g. blind via prepreg.

Materials for flexible circuits specified to Military Specifications or with unspecified materials shall be in accordance with IPC-6013. The following materials may be used:

1. Flexible Base Dielectrics per IPC-FC-231/1

2. Adhesives, Adhesive Coated Dielectric Films, and Flexible Adhesive Bonding Films per IPC-FC-232/1, /18 or /21.

3. Flexible Metal-Clad Dielectrics per IPC-FC-241/1 or /11

For rigid boards, foil shall be in accordance with IPC-MF-150/1 or /3. For flexible circuits, foil shall be in accordance with IPC-MF-150/7. Foil treatments are left to the discretion of the supplier, provided performance characteristics are met for the completed board. The copper weight and/or thickness on the PWB drawing represents the finished dimension.

3.2 FINISHED THICKNESS AND OUTLINE DIMENSION TOLERANCES

Thickness shall be as specified on the PWB drawing, but the tolerance shall be no tighter than ±0.005”. Tolerances for outline dimensions for flexible circuits shall be no less than ±.010”.

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3.3 CONSTRUCTION

For rigid boards, the board layer stack-up is specified on the PWB drawing. Unless specified on the PWB drawing, 1 oz internal copper foil shall be used. Unless otherwise specified on the drawing, the finished external copper layer thickness shall be equivalent to 1 oz (0.0012") minimum. Where construction method is specified on the PWB drawing, traditional, foil, or cap construction is acceptable provided dimensions in the layup diagram are met. If foil construction is utilized, foil shall be in accordance with section 3.1; and foil adhesion must meet the performance requirements of the corresponding clad laminate. Unless otherwise specified on the drawing, the dielectric spacing between copper layers shall be 0.0035" minimum (reference see Figure 3-14 of IPC 6012B).

For flexible circuits with stiffeners without plated through holes, the hole size on the stiffener shall be the diameter of the corresponding pad. If the pad is not circular, the stiffener hole diameter shall be equal to the largest feature of the pad, e.g. the long dimension for oval pads or the diagonal of a square pad.

For flexible circuits with stiffeners and plated through holes, the stiffener may be attached to the flexible circuit before or after hole plating. When desired for manufacturability, the stack-up may be modified to include stiffeners on both sides of the flexible circuit, each one half the specified stiffener thickness. Bonding may be accomplished by the use of acrylic adhesives or prepreg. A protective layer (e.g. "pouch"), to be removed from flexible areas of the circuit, may be added to the stack to prevent degradation of the circuit/cover slip during wet processing. The total stack-up must be within the overall thickness tolerance specified on the PWB drawing, and the resultant plated through holes shall meet the requirements of §3.4.2. All materials used shall be in accordance with § 3.1. (See Figure 1.) AMETEK shall be notified of the supplier's intent to utilize this construction prior to fabrication of product.

Flexible circuits with any type of stiffener shall have a stress relief adhesive fillet at the rigid/flexible interface extending 75% up the stiffener thickness minimum, and .080" or 150% of the stiffener thickness, whichever is greater, maximum on extending out over the flexible board's surface. The adhesive shall be Ecobond 45 or equivalent.

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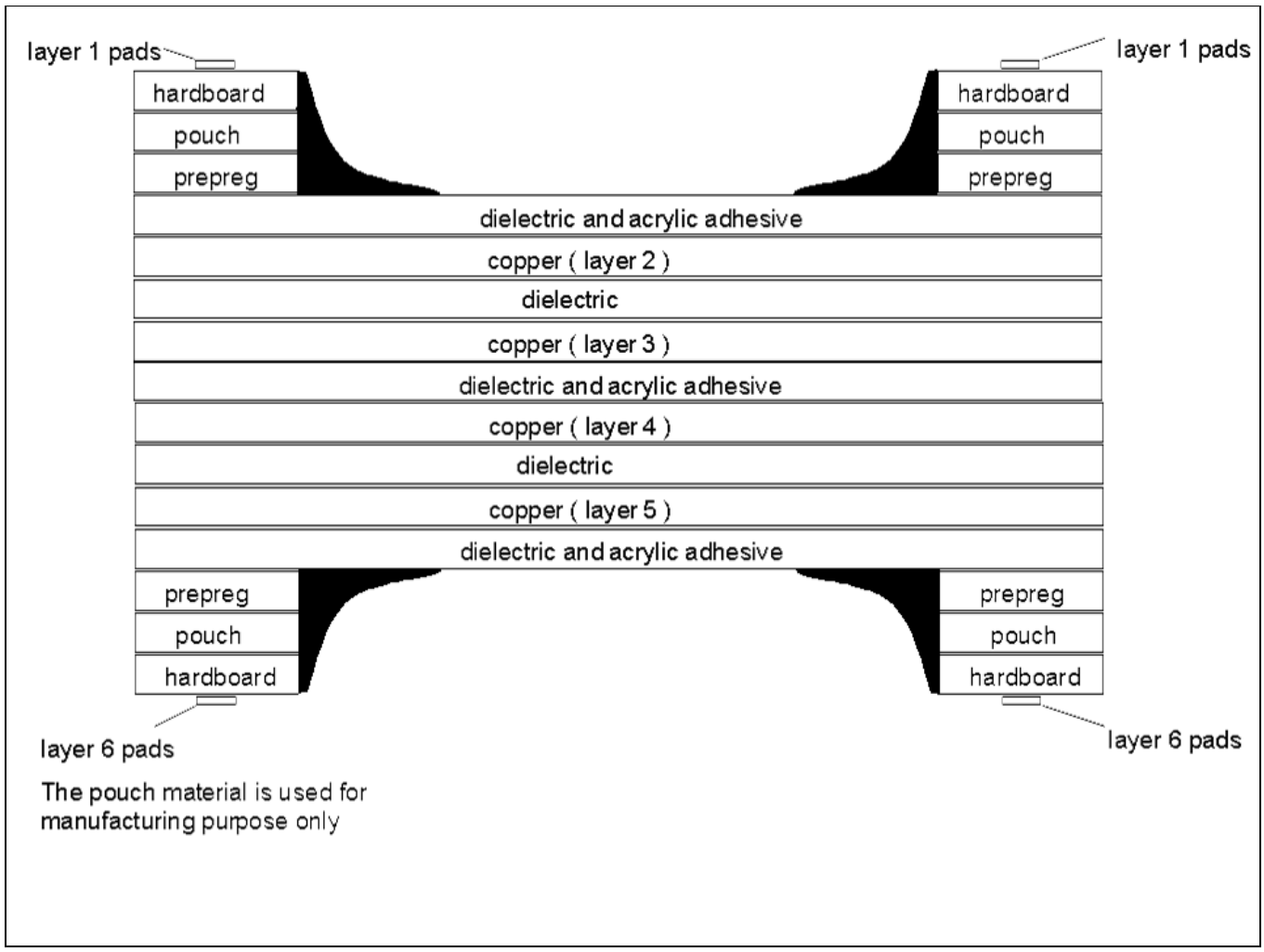


Figure 1. Sample of Flexible Circuit Construction with "Sandwiched" Plated Through Hole Stiffeners.

Note: This example utilizes adhesiveless copper clad flexible substrates and prepreg stiffener attachment options. Acrylic is used for all the other adhesive materials. Pads for layers 1 and 6 are the same dimensions as the corresponding pads for layers 2 and 5, respectively.

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3.4 HOLES

3.4.1 HOLE SIZE

The number and finished (plated) size of all holes is specified on either the PWB drawing or the Drill Tape file. Finished hole tolerance is +/- 0.003" unless otherwise specified.

Holes that are listed as size "PLATED CLOSED" are to be made as large as reliably possible given the pad size on the design. Considerations such as aspect ratio, layer to layer registration, and drilling accuracy must be taken into account. The finished hole size is not critical and can be of any size, down to totally blocking the via; however, to reduce the likelihood of entrapping fabrication chemistries, plating vias closed is discouraged.

3.4.2 HOLE PLATING

All holes on rigid boards and flexible circuits except those shown with locational dimensions on the PWB drawing, or holes specifically noted as nonplated, are to be plated through with electroplated copper per IPC-6012 and IPC 6013 as applicable with the following exceptions:

Electroless copper plating or direct metalization processes may be used to form a conductive surface within the plated through holes per IPC-6012 and IPC-6013, as applicable, except the graphite based "Shadow" process shall not be used without written authorization of AMETEK Design and Supplier Quality Engineering.

3.4.3 BLIND AND BURIED VIAS

Controlled depth drilling shall not be performed to form blind vias. All blind and buried vias shall be formed using the sequential lamination method.

3.4.4 VIAS IN SMT PADS

All plated through vias within surface mount component pads must be plugged using an approved Via Plug Polymer in a manner consistent with the manufacture's guidelines. Via holes to be plated prior to plugging in accordance with IPC-6012.

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3.5 SOLDER MASKS

Photoimageable per IPC-SM-840, class H. Color Green unless otherwise specified. Either wet or dry photoimageable can be used for PWB's with no surface mount pads. Liquid photoimageable solder mask shall be used with surface mount boards. All solder masks are to be applied SMOBC (Solder Mask Over Bare Copper).

Liquid cover coats are not permitted on flexible circuits.

3.5.1 SOLDER MASK APERATURE SIZE

Apertures for solder mask gerber files may be designed with or without manufacturing allowances. In some cases the apertures are 1:1 to the pads, while in other cases the apertures are large enough to expose adjacent conductors if not registered precisely with the circuit artwork.

The supplier shall modify the solder mask apertures to be optimized to the supplier's process capabilities. The resulting mask shall meet IPC-6012 registration requirements (Class as defined in 3.0), and shall not expose adjacent conductors, including via pads.

3.5.1.1 TENTED VIAS

Solder mask apertures for vias that are smaller than the pad diameter are intended to be tented (i.e. pad is covered, but not plugged). Note that both sides of the same via hole might not be tented, as one side may be used as a test point. Tented vias do not have to be plugged.

3.6 CONDUCTIVE PATTERNS

Artwork/gerber data supplied represents the nominal conductor widths required. When not specified on the fabrication drawing, the minimum conductor width shall be 80% of the conductor pattern supplied in the artwork or data. In no case shall the conductor width be less than 0.005". The conductor spacing, if not specified on the PWB drawing, is allowed a reduction of up to 20% in the nominal conductor spacings shown in the artwork or data. In no case shall the conductor spacing be below 0.005". This absolute minimum is applicable for both the internal and external conductors.

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Modification of the supplied artwork/gerber data to account for manufacturing allowances is acceptable. Otherwise, conductive patterns shall not be modified in any way that results in a finished product that does not conform to the original artwork/gerber data with tolerances as defined by IPC-6012 and IPC-6013.

"Fillets" or "keyholes" may be added to pads to reduce the likelihood of trace/pad junction breakout as long as the enhancements do not reduce nominal conductor spacing beyond the minimum spacing provided by the design.

All outer layer conductor patterns shall be plated with copper per IPC-6012 or IPC-6013, as appropriate.

3.7 STANDARD CONDUCTOR FINISH

All boards, outer layers and plated through holes, shall be HASL (hot air solder leveled) with Sn63A, per J-STD-006, and in accordance with IPC-6012 or IPC-6013 as applicable. The PWB drawing will specify nickel and gold plating if required. All boards are to have NO tin-lead plating under the solder mask or cover-slips for any reason (within the limits of IPC-6012 and IPC-6013 for solder wicking).

The use of Organic Solderability Preservatives, Flash Gold platings, White Tin, or other coating with the purpose of solderability preservation is prohibited unless written approval is obtained from AMETEK, Aerospace Engineering.

3.8 SELECTIVE GOLD PLATING

When specifically noted on the PWB drawing, indicated areas are to be plated with electrolytically deposited Gold over Low Stress Nickel plating. Nickel plating shall be per IPC-6012, except when noted as ".000150 in. minimum". Gold plating shall be in accordance with ASTM B488-95, Type 3, hardness code C or D with thickness per IPC-6012. Electroless Gold plating processes cannot be used unless evaluated and approved by AMETEK, Aerospace Engineering.

Where plated through holes are included within the selective gold area, the intent is to have contact surfaces gold plated only (e.g. zebra strips). Some PWB drawings specify for one entire side of the board to be gold plated, while the other side and PTH barrels shall be solder plated. In these circumstances, the contact surfaces such as zebra strips and goldfingers **shall** be selectively gold plated; solderable

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surfaces such as PTH pads **shall** be solder coated per § 3.7 and tented vias and traces **should** be SMOBC; however, gold plating under the solder mask is permissible.

3.9 SILKSCREEN

White epoxy, heat resistant nonconductive ink per IPC-6012. When HYSOL 10-105 or equivalent is specified on the PWB drawing, HYSOL 10-105 must be used in the areas indicated on the detail. The ink must be applied twice. Each application must be followed by a curing cycle.

Note: Boards requiring HYSOL 10-105 ink have special light reflectance and transmission requirements. No substitutes may be used.

3.10 VERSION MARKING

The boxed letter etched in copper on the noncomponent side of the PC board is the current artwork version. Where revision boxes do not exist, the last three digits of the part number control the configuration, e.g. B1619-xx-003 refers to configuration 003.

3.11 SUPPLIER TRADEMARK AND DATE CODE

All multilayer printed boards and multilayer flexible circuits shall contain supplier trademark, date code, and if possible or if requested, serial numbers. Single and double sided printed boards and flexible circuits shall have only the supplier trademark and date code. They shall be placed on non-component(secondary, or bottom) side where space permits, or on the reverse side if necessary due to space availability. Date codes shall indicate week and year. All markings shall be ink stamped, etched, or screened. Ink stamping shall be per paragraph 3.9 above. As specified in IPC-6012, the serial number of the board, if applicable, shall be traceable to the panel, all coupons, and mounted sections. Etched markings must be 0.050" minimum from any other conductor, and shall not be within component foot prints indicated by silkscreen.

3.12 INSPECTION AND TEST AT SUPPLIER

3.12.1 ELECTRICAL TEST

Each and every multilayer raw board and flexible circuit shall be 100% tested by the printed board supplier for electrical shorts and opens. Designs including Surface Mount Technology must be tested using a fixture or method that is

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capable of testing both sides of the board simultaneously. Single and double sided rigid boards, and single layer flexible circuits are exempted from this requirement unless specifically noted on the PWB drawing or purchase order. The test voltage must be twice the rated voltage of the board as specified on the PWB drawing. If not specified, the test voltage must be at least 40V. Test shall be in accordance with IPC-9252, IPC-6012, and IPC-6013 as applicable. For continuity there shall be no open circuit whose resistance exceeds 10 ohms. For referee purposes, 0.5 ohm maximum per inch of circuit length shall apply. For shorts test, the resistance between mutually isolated conductors shall be greater than 10 megohms. Each board must be tested 100% for continuity and shorts as specified in IPC-6012 or IPC-6013 as applicable.

Multilayer rigid boards and two or more layer flexible circuits shall be tested to the provided CAD net list. If no net list is provided, the boards shall be tested to a net list generated from the gerber data. If Ametek or the supplier can not generate gerber data, a Golden board test may be used.

Test fixtures and programs shall be developed using IPC-9252 as a guideline. Probes must be appropriate for the surface contacted, such that the surface is not damaged and the contact is adequate.

3.12.2 AOI INSPECTION

Automated Optical Inspection (AOI) when used in lieu of visual inspection must compare the panel to scanned artwork or CAD data. Design rules may not be used as the sole criteria. When utilized, AOI shall be performed using IPC-AI-642 as a guideline.

3.12.3 ACCEPTANCE TESTING

Acceptance testing and frequency shall be performed in accordance with the latest revision of IPC-6012 or IPC-6013 as applicable.

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Inner-layer breakout is not acceptable in cross-sectioned coupons of multilayer panels. In order to accept the panel, objective evidence must be maintained by the supplier that no internal trace-pad junctions have been broken out, and that trace widths have not been reduced more than 20%. This may be accomplished by means of additional cross-sections, F coupons, X-ray analysis, etc. (see par 3.6.2.9 of IPC-6012B).

On double sided boards (type 2) only, coupon A or coupon B which contains the smallest diameter hole shall be thermal stressed and micro-sectioned. Potted micro sections on type 2 boards are not required to be sent with shipments; however, must be retained for recall by AMETEK for a minimum of 3 years.

One printed board or flexible circuit is required to be tested for ionic cleanliness prior to shipment after all operations have been performed on the board, even if the item has been in stock. Cleanliness must also meet the pre solder mask cleanliness requirements of IPC-6012 or IPC-6013. All ionic cleanliness tests, both prior to solder mask and after the final board operation , must be recorded on a log sheet and kept on file. The test data shall be traceable to the part number, serial number (if applicable), or date code and the date tested along with the acceptance readings. It shall be readily available if requested by AMETEK. One board per order must be inspected 100%(using pin gauges for the proper hole sizes). Also 1 board per order must be inspected for all dimensions on the outlying drawing if applicable.

3.13 DATA REQUIREMENTS

Supplier must check all documentation and purchase order requirements to make sure they match before building any PWB. If they don’t match they must contact purchasing at Ametek.

Supplier shall issue a C of C (Certificate of Compliance) with every shipment. A First Article inspection must be issued with every first-shipment or a shipment that includes a rev change that effects the outline configuration or dimension. The supplier must record the minimum average copper plating thickness of the PTH’s (plated through holes) on the C of C or on a separate data sheet attached to the C of C. Also included on the C of C is the list of all the serial numbers of the boards (if applicable) shipped in the lot. Solderability shall be certified to J-Std-003 and the test must be appropriate for the technology of the board as

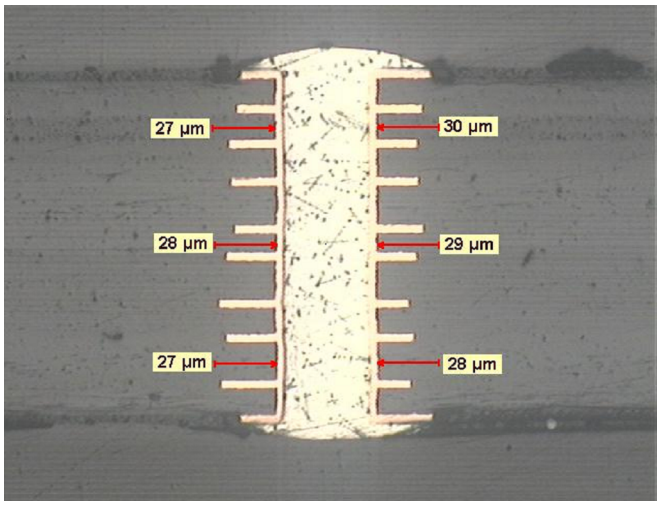
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specified in J-Std-003. A scrap board from the lot may be used and preferred as a sample(don't send this board to Ametek).

Unless otherwise specified in writing by Ametek's Quality Engineer, all solder stressed samples must be stored at the supplier for 3 years. Digital pictures of a large and small hole(solder stressed at 280C) for each panel shall be sent with the test report showing the copper thickness measurement if requested. Each image if supplied must be identified to the item's part number, supplier, date code and serial number if applicable.

Cross section data shall be submitted with each shipment. The data must include part number, supplier, and date code. Cross section data not required with shipments of single and double sided rigid boards, or single layer flexible circuits.

Test data (EOL yield) by serial number if applicable must be supplied with each shipment. Cross section parts and all associated build information must be retained for 3 years.



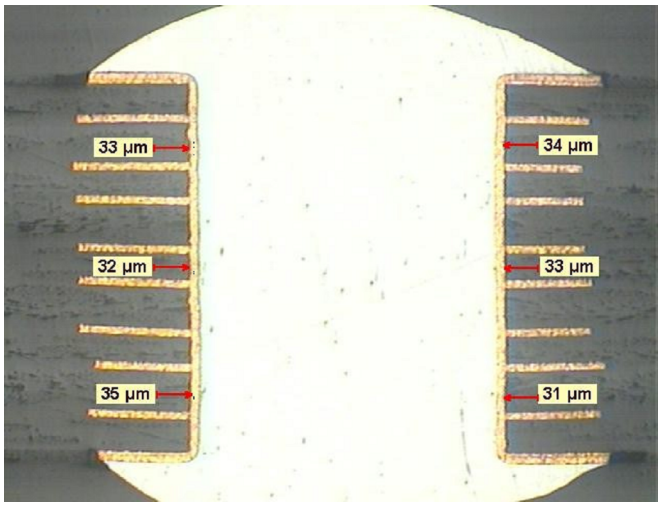


Figure 2. Samples of digital pictures of small and large hole cross sections.

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3.14 PACKAGING

Each finished board shall be placed in an individual polyethylene bag (or equivalent)or you may stack up to ten boards in a polyethylene bag or equivalent. The only exception is lead free boards they must have sulfur free paper interleaved between layers. Each bag or group of bags along with appropriate number of desiccant bags must be sealed to prevent moisture and or contamination getting into the sealed bags. The bag shall be marked with an AMETEK part number, date code and PWB drawing rev level.

No more than one or 10%, whichever is greater, of multi-board arrays may contain X-outs. No more than one X-out is permitted per array.

4.0 SUPPLIER SELECTION

Boards are procured from approved sources based upon the supplier's capability. All supplier issues dealing with criteria should be addressed per attached engineering sheet (or equivalent) to the appropriate design Engineer. See Figure 3.

AEROSPACE AEROSPACE & DEFENSE
33 Lewis Rd Binghamton, NY 13905-1045
Telephone: 607-763-4700 Fax: 607-763-4717

To:						Customer Name:	AMETEK
Cc:						Customer Part No.:	
From:						Supplier Part No.:	
Date:						Telephone:	

ENGINEERING INQUIRIES

	Descriptions	Suggestion	Reply & Signature
	General		
1			
2			
3			
4			

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