

Industry Roadmap and Technology Strategy

Martin van den Brink

President and Chief Technology Officer

Industry Innovation

- Moore's law innovation continues, driven by multiple engines of performance scaling which is expected to accelerate over the next decade
- Continued process technology innovation attracts new applications and increases wafer volume

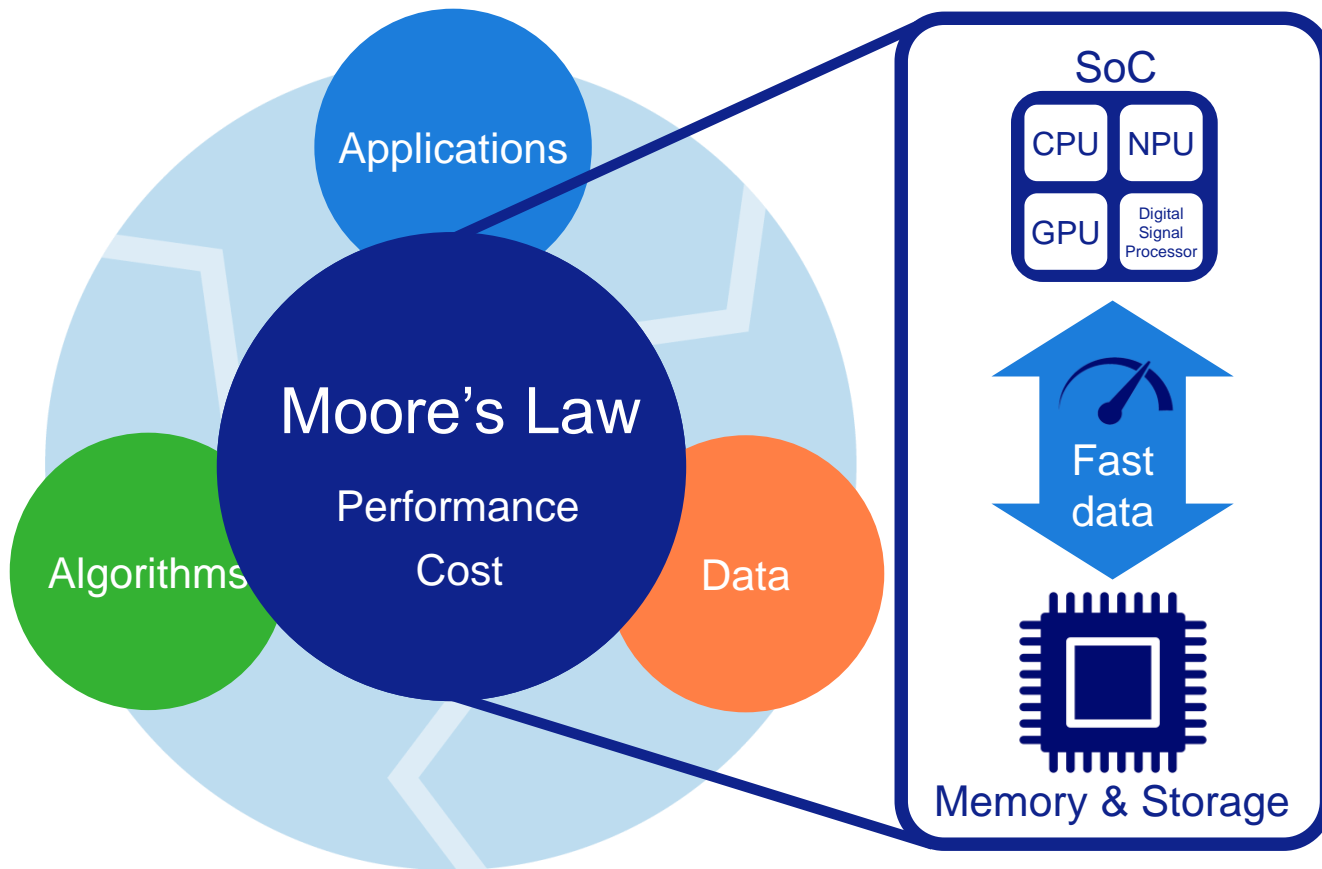
Customers' Roadmap

- Customers' roadmaps require lithography enabled shrink beyond next decade
- Higher wafer volumes at leading edge nodes drive a continued demand for higher productivity, lower cost and simpler processes

ASML's Holistic Litho Solutions Roadmaps

- Our product portfolio is aligned to industry trends and customer requirements with a detailed product roadmap
- Execution of our strategic priorities will provide required solutions for our customers, enabling cost effective shrink beyond the next decade

Major trends in semiconductor-enabled computing

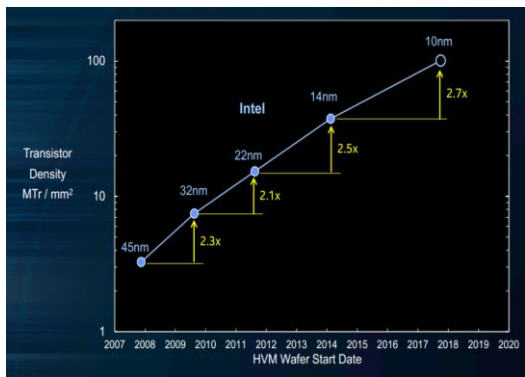


Moore's Law innovation continues

Driven by multiple engines of performance scaling

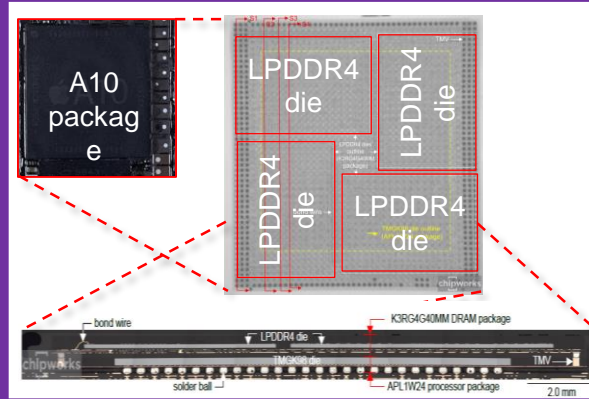
Dimensional Scaling

Patterning and circuitry shrink



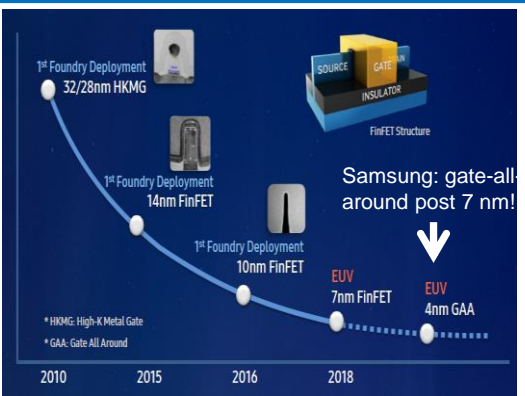
Circuit scaling

3D, System-on-chip and advanced packaging



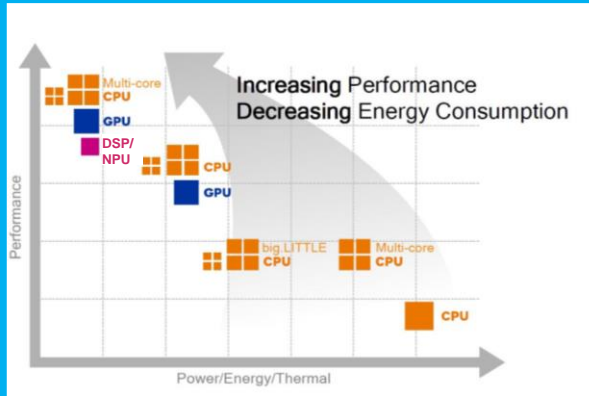
Device scaling

New devices and materials



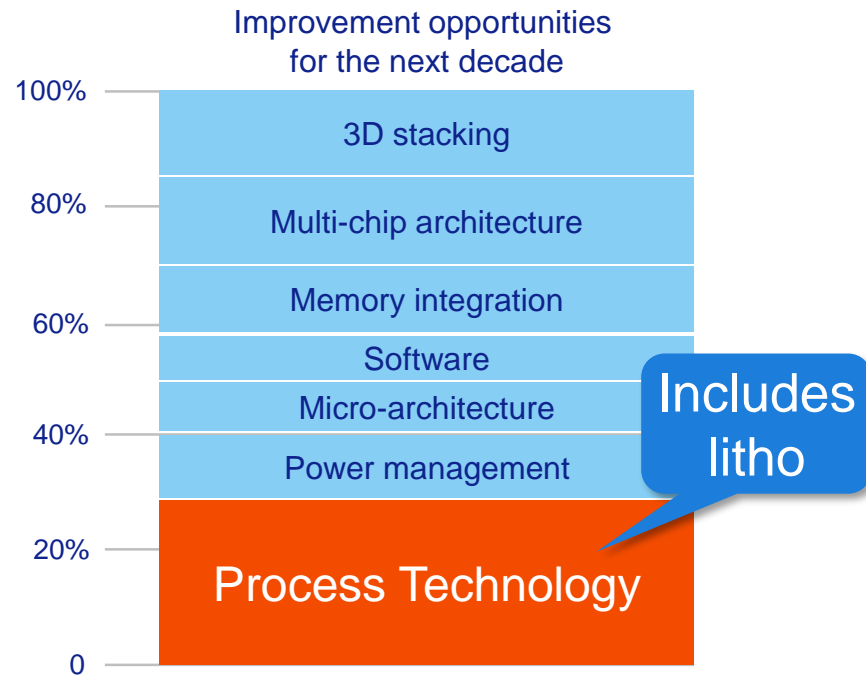
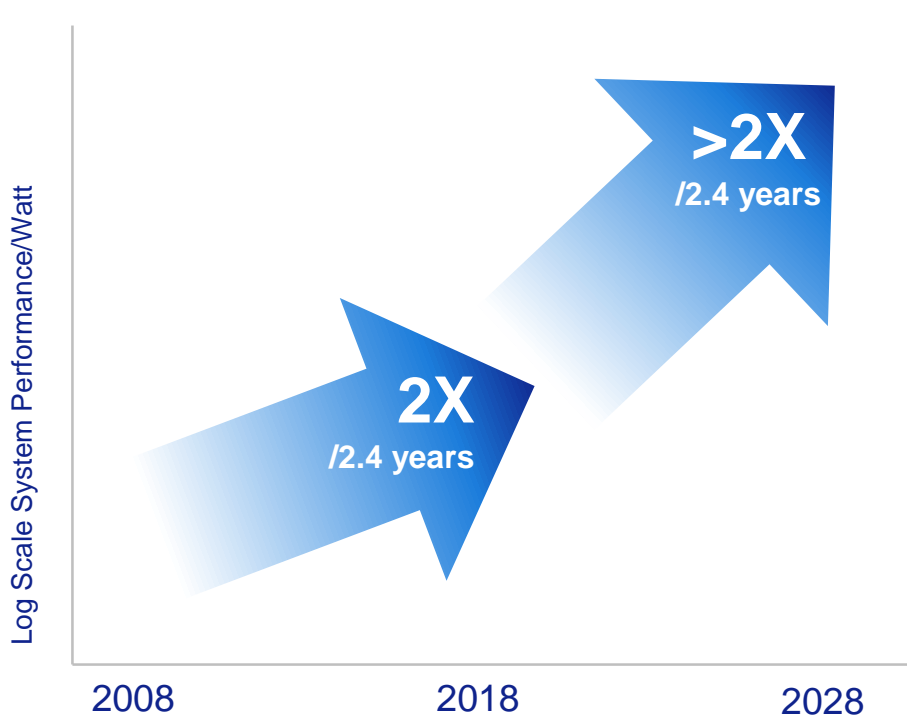
Architecture scaling

Solution optimization



Chipmakers accelerate performance for the next decade¹

Process technology innovation accounts for 30% on par with Moore's prediction²



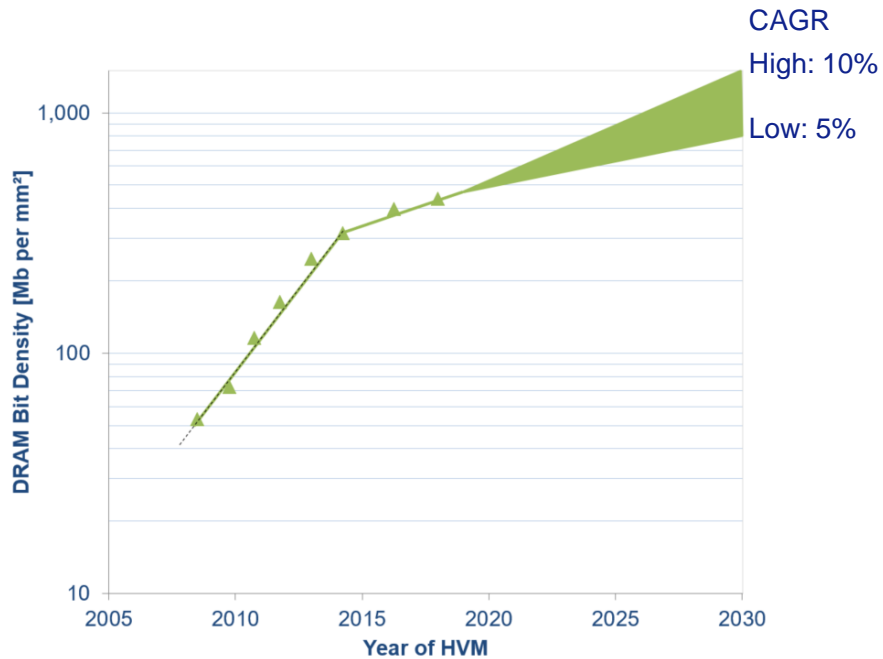
¹Lisa Su, AMD, "Immersive era in consumer computing", IEDM, dec 2017

²Gordon Moore, "Progress in digital integrated Electronics" International; Electronic Device Meeting, IEEE, 1975, p p 11-13

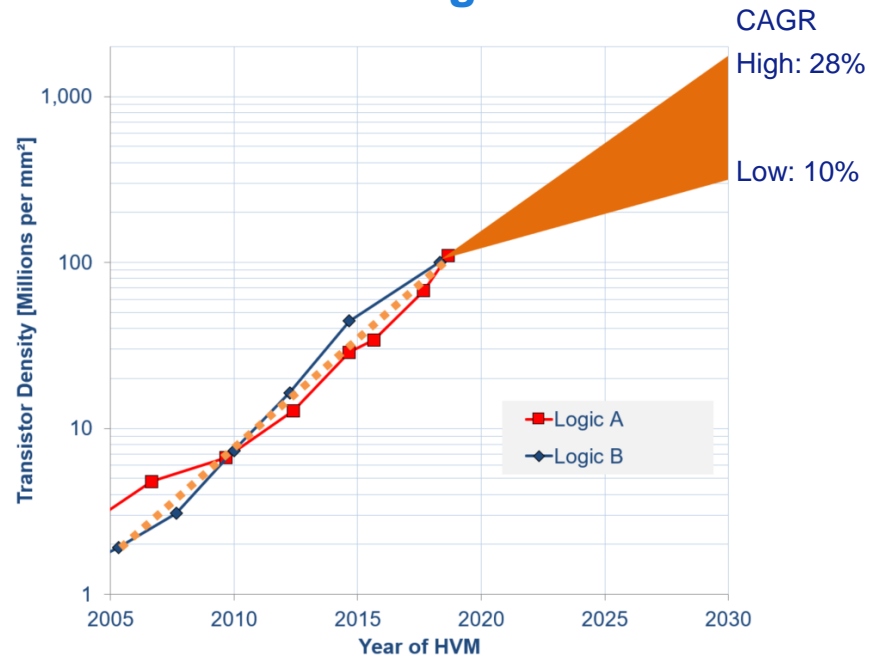
Customers' roadmaps show continued need to shrink

ASML's roadmap aligned to deliver solutions

DRAM

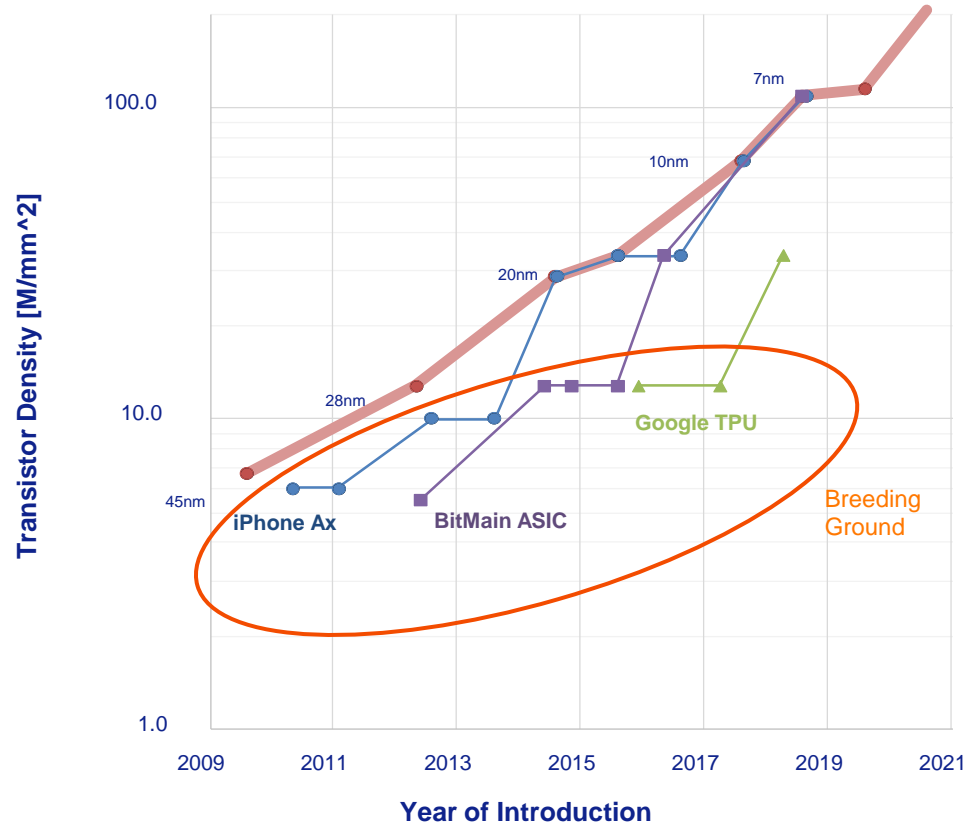


Logic



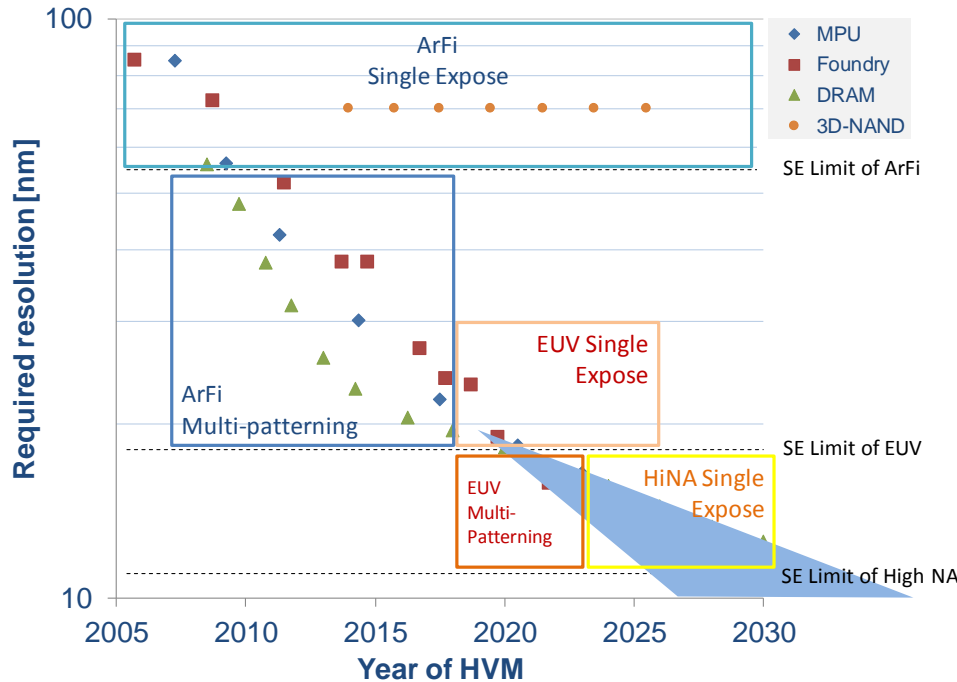
Innovation attracts new applications

Starting at trailing nodes and migrating fast to leading edge



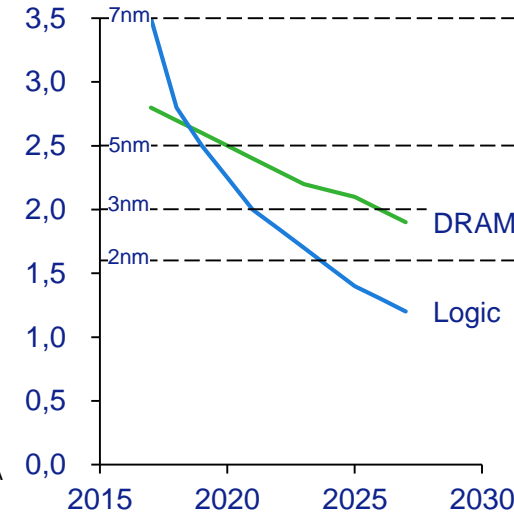
Combined EUV, High NA, DUV and holistic solutions needed to support shrink in the next decade

Minimum resolution continues to shrink ...



... and Logic takes over from DRAM in overlay scaling

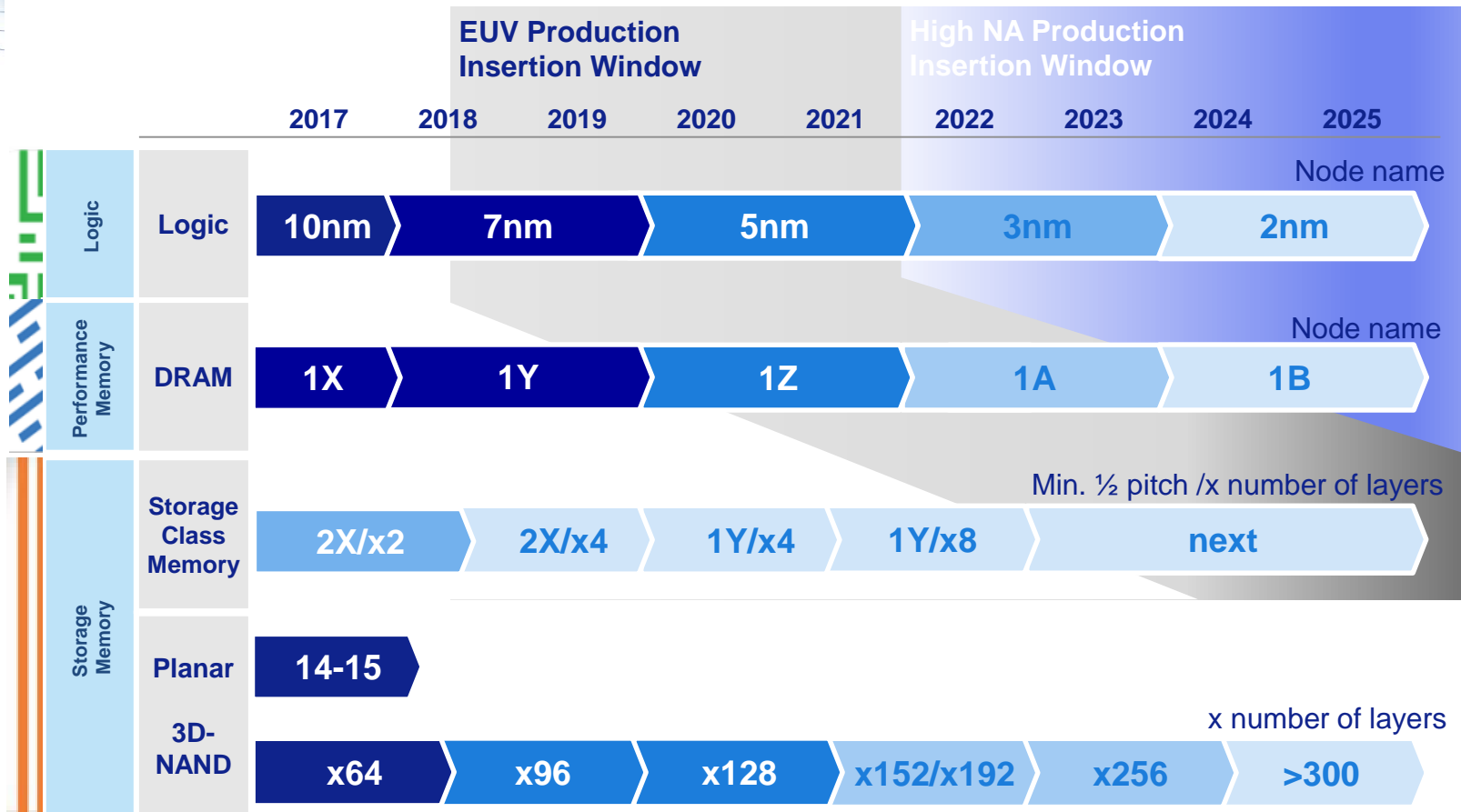
On Product Overlay [nm]



Mix&match lithography	Applications
NXT:1980i NXE:3400B	YieldStar Software
NXT:2000i NXE:3400C	YieldStar Software
ArFi Next NXE:3400C	YieldStar Software
ArFi Next NXE Next	YieldStar Software

Customers request complementary product innovation

Customers' scaling roadmaps continue



Source: ¹ Customers public statements, IC Knowledge LLC; ² ASML extrapolations

Our strategy to enable shrink

Holistic Litho extension

- Strengthen Litho+ leadership with **in device metrology** enabling correction of process induced overlay
- Build a winning position in **Pattern Fidelity Control** leveraging e-beam metrology and inspection combined with superior computational Litho and fast stages

DUV performance

- Drive **DUV performance**
 - Continue to lead in innovation
 - Drive operational cost down and improve up-time
 - Expand installed base business

EUV industrialization

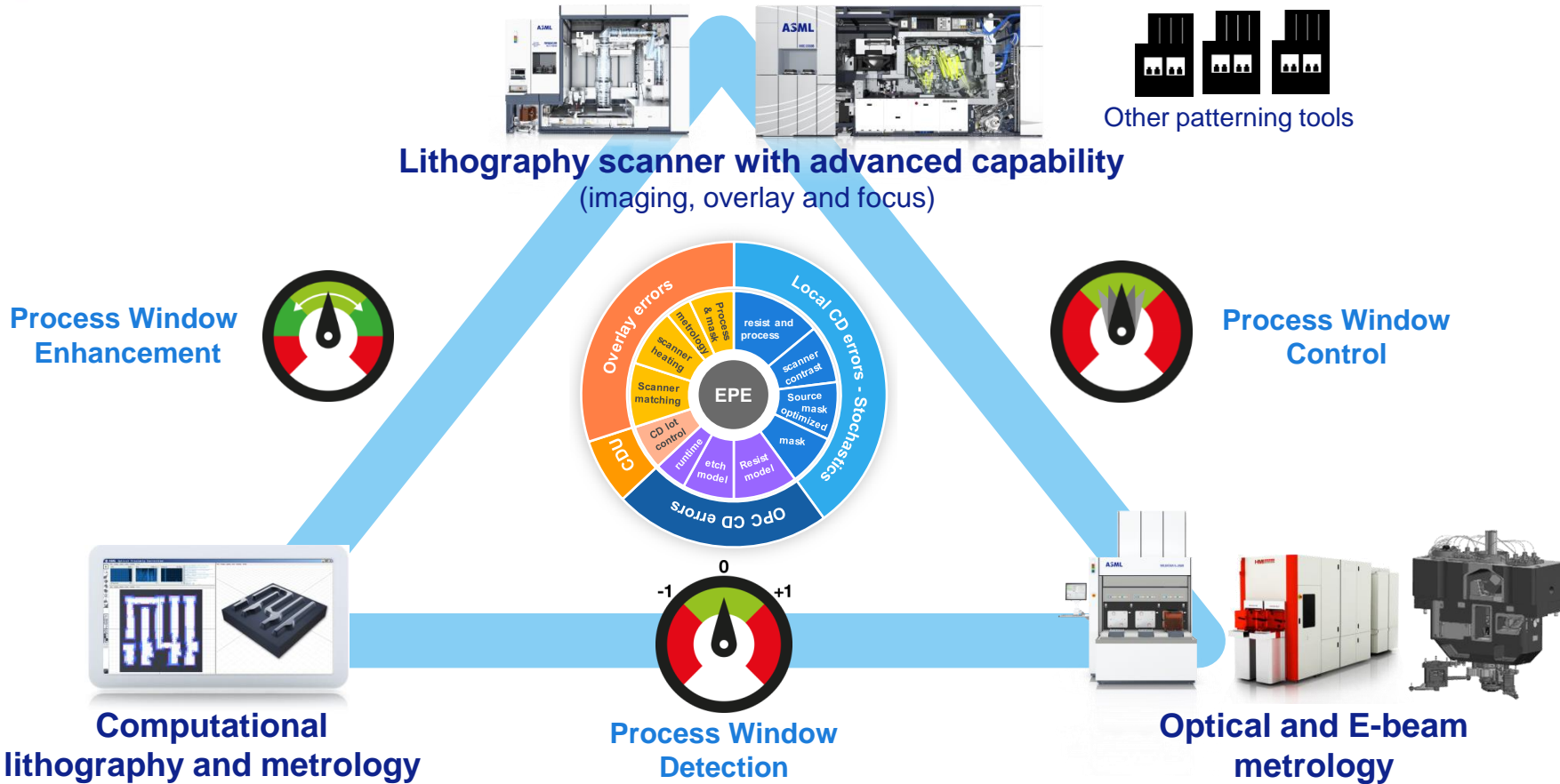
- Deliver on **high volume manufacturing, service and financial** performance
- Enhance EUV value for future nodes by **extending NA 0.33 product portfolio down to the 3nm Logic node**

High NA

- Enable **High NA EUV** at 3nm Logic node, followed by memory nodes at comparable density

ASML's Holistic Lithography roadmap optimize

patterning performance through patterning, metrology and computational integration

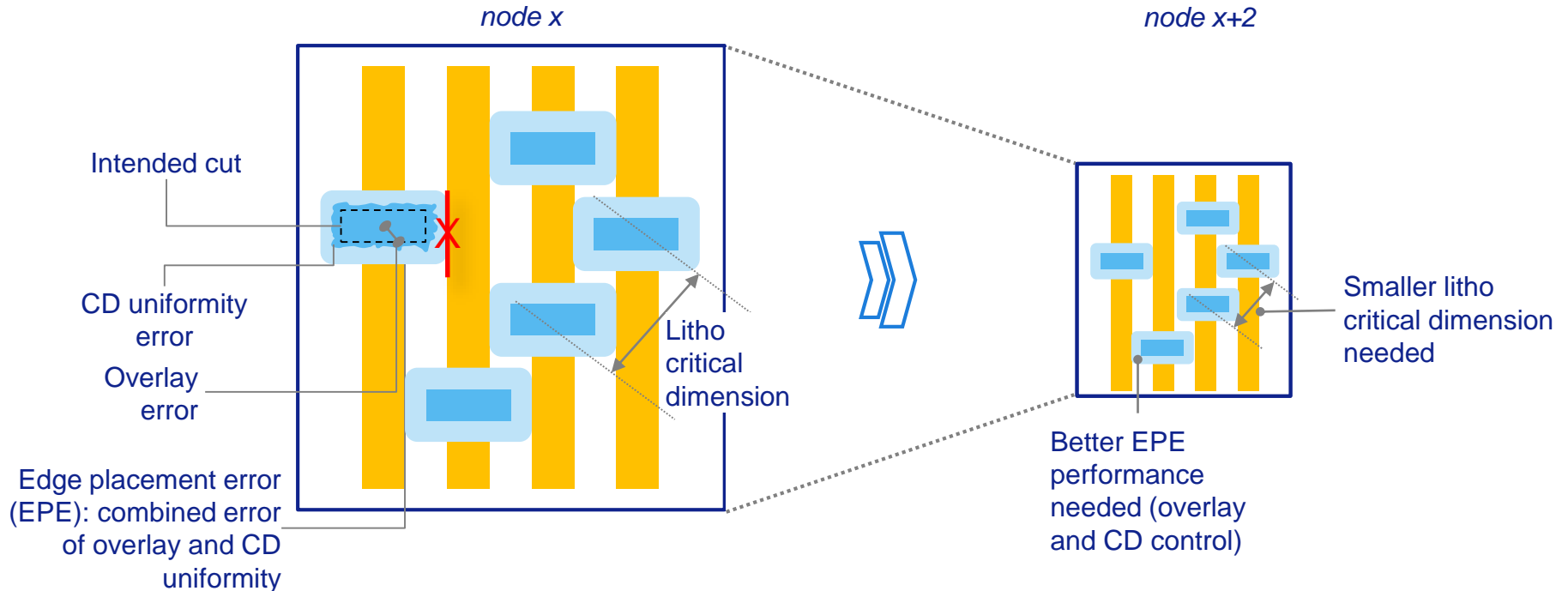


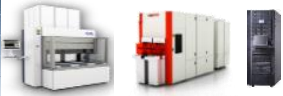
Main factors for continued shrink

Edge placement error and shrinking litho critical dimension

Edge placement error (EPE) and litho critical dimension (CD) main patterning parameters...

...and shrink requires ever tighter requirements

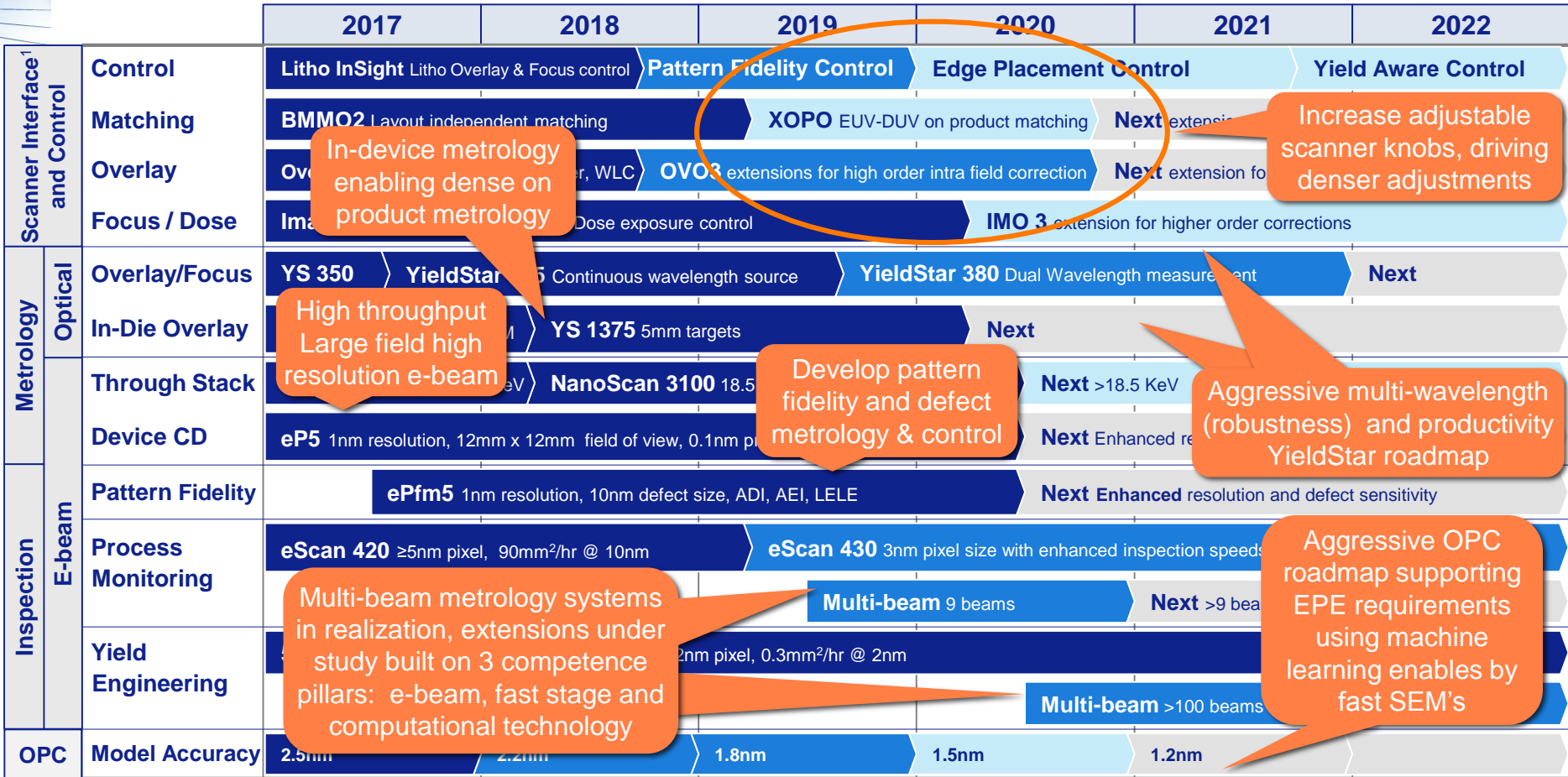




Applications Product Roadmap



ASML



In-device metrology enabling dense on product metrology

Increase adjustable scanner knobs, driving denser adjustments

High throughput Large field high resolution e-beam

Develop pattern fidelity and defect metrology & control

Aggressive multi-wavelength (robustness) and productivity YieldStar roadmap

Multi-beam metrology systems in realization, extensions under study built on 3 competence pillars: e-beam, fast stage and computational technology

Aggressive OPC roadmap supporting EPE requirements using machine learning enables by fast SEM's

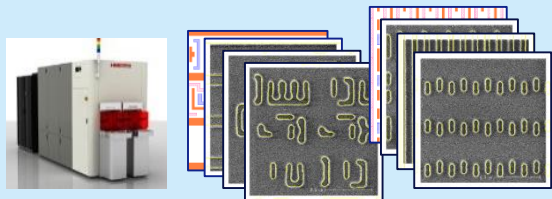
¹ Timing and functionality for NXT interfaces, NXE timing & functionality differ; BMMO: Baseline Matched Machine Overlay; WLC: Wafer Level Control; MAM: Move-Acquire-Measure, OPC: Optical Proximity Correction, 2D CD accuracy 3s

Better accuracy of lithography models by deep learning

Enabled by fast e-beam metrology and physical based models

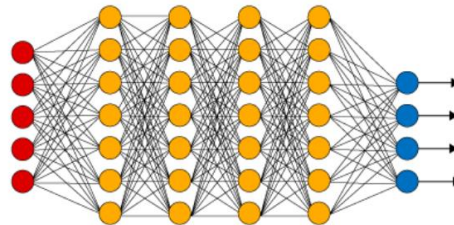
Accuracy

Data-driven **training** based on fitting spec and wafer measurements



Large volume wafer metrology data, further enhanced by fast e-beam

ASML Deep learning model

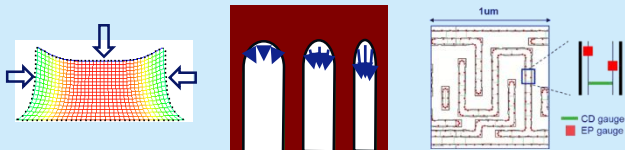


Captures complex effects required by the data

Feature extraction:
Final resist model trained does not contain human-engineered model terms and achieves better **accuracy**

Stability

Physical driven **training** using physics based lithography models



Physical Resist Shrinkage

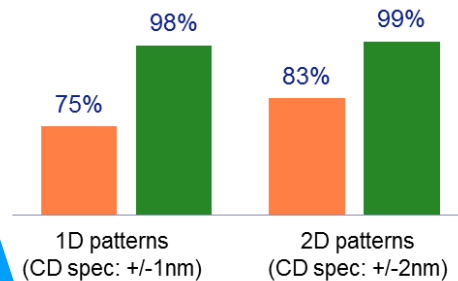
Resist surface stress

Data expansion through simulated contours

Example 1

Percentage of patterns within accuracy spec

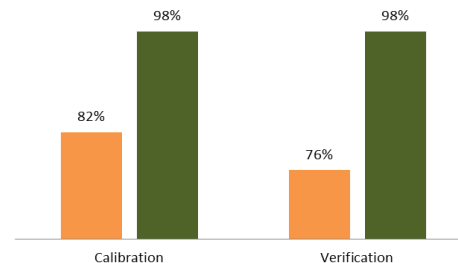
■ Baseline ■ Machine Learning



Example 2

Model Accuracy: Percentage of gauges within spec

■ Physical Based NTD ■ Machine Learning

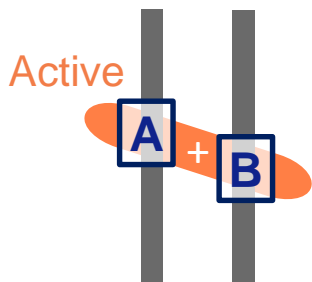


Yield Star In-Device Metrology improves electrical yield

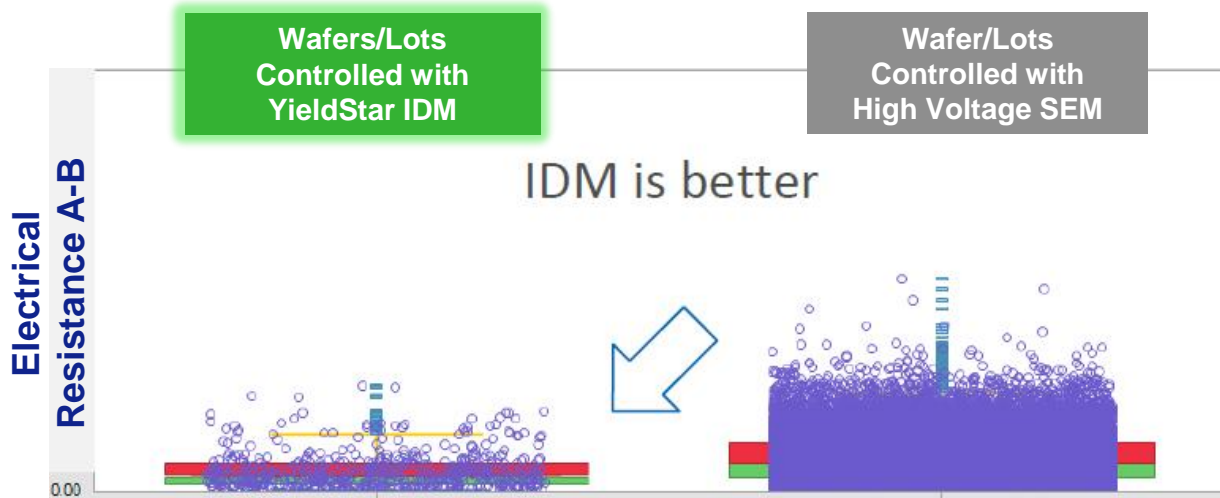
Compared to SEM on word line DRAM layer

Electrical Resistance Test
 $A-B = 0 \rightarrow$ Zero Overlay

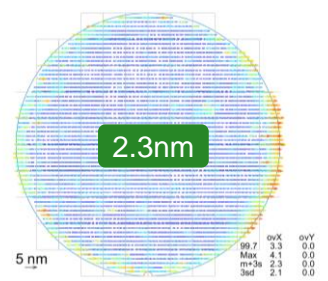
DRAM Memory Cell



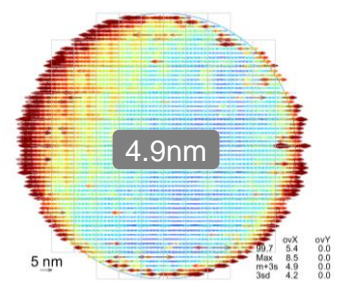
Word Lines



Overlay fingerprint after IDM Control



IDM measured overlay fingerprint after SEM Control



Applications: expanding solution space

Drives growing product portfolio

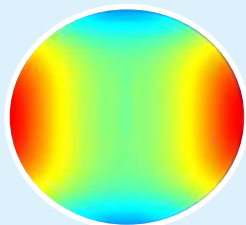
Computational Lithography

- Deep learning and fast e-beam metrology (HMI) differentiate our model accuracy
- Better accuracy enables wafer defect prediction, enabling higher speed inspection



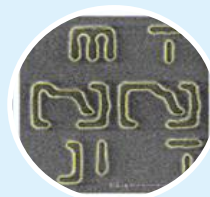
Optical Metrology

- Entering growing after-etch in device overlay market with YS:1375
- Opening new use-cases with machine learning, instead of reconstruction



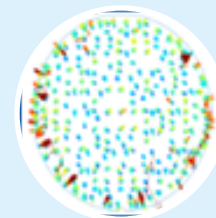
E-Beam Metrology & Inspection

- Expanding CD-SEM opportunity
- Process Window Qualification opportunity for e-beam inspection
- Progressing high productivity multi-beam roadmap



Process Control

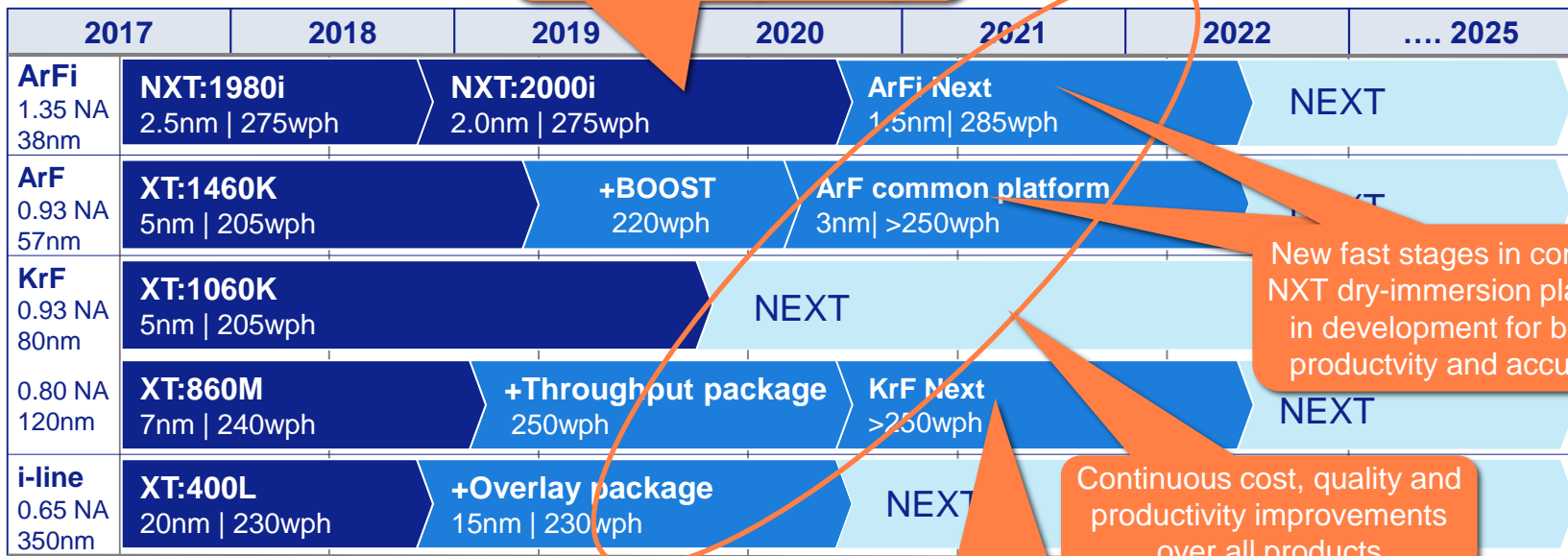
- Process control solution running in volume production
- Focus on process control market dynamics aligned to value of yield-based control



DUV Product Roadmap

Extending throughput for cost reduction and overlay for yield improvement

Key immersion innovations in alignment, wafer table and level sensor synced with NXE for tighter overlay matching



New fast stages in common NXT dry-immersion platform in development for better productivity and accuracy

Continuous cost, quality and productivity improvements over all products

XT enhancements to address 3D NAND requirements

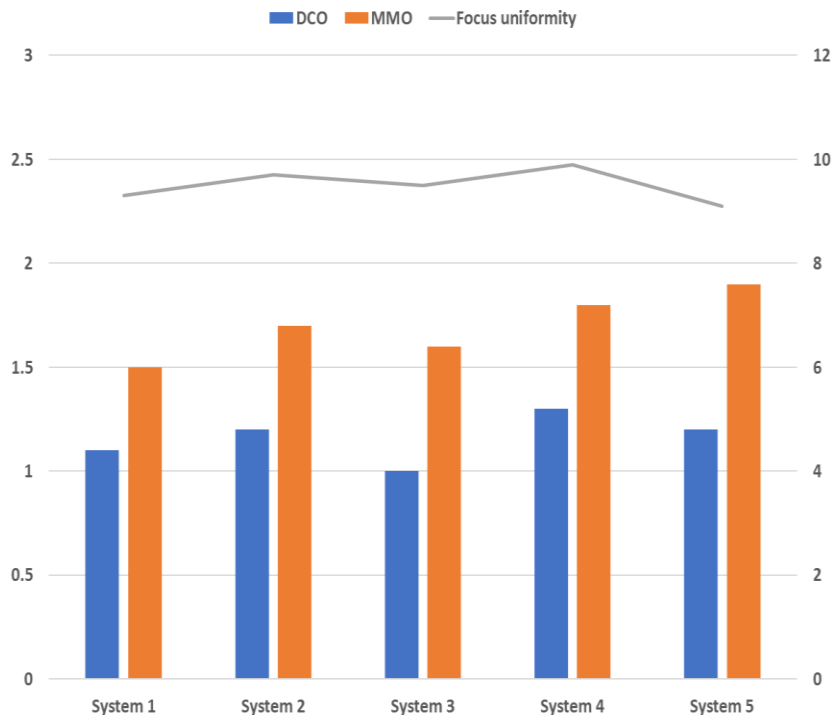
Product
Matched Machine
Overlay|Throughput

Current Product status

- Released
- Development
- Definition

NXT:2000i performance exceeding expectations

As measured on multiple systems shipped



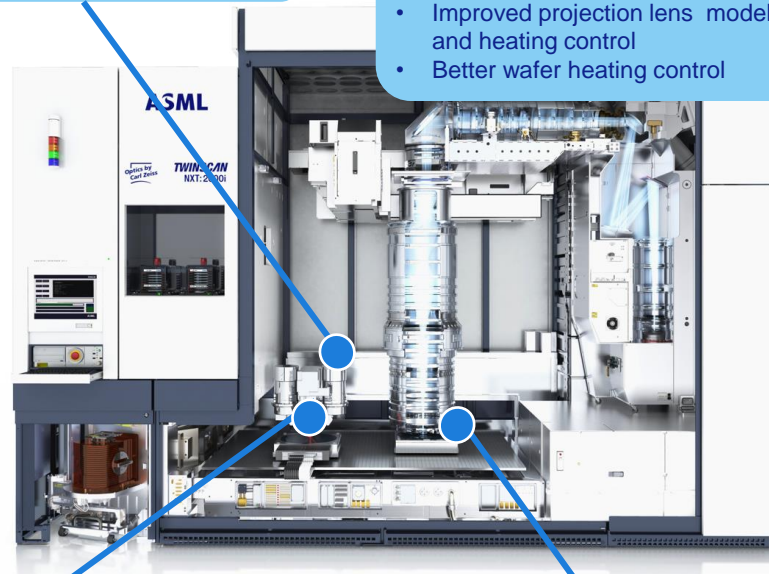
DCO: Dedicated Chuck Overlay
MMO: Matched Machine Overlay

Alignment sensor

- More process robustness
- Higher yield

Additional features

- Improved grid setup for better overlay and calibration
- Improved projection lens modeling and heating control
- Better wafer heating control



Level sensor

- Reduced process dependency
- Improved matching

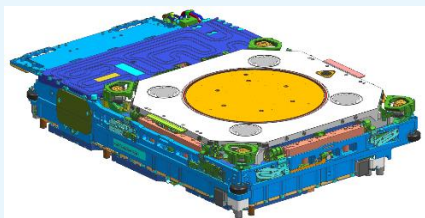
Wafer Table

- Improved matching to EUV
- Improved flatness & endurance

DUV: mix and match with EUV and drive to perfection

Innovation Leadership

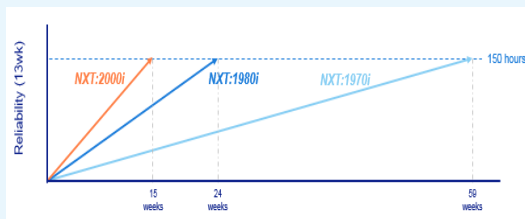
- Leadership in Immersion with the NXT:2000i featuring a next generation alignment sensor, focus & levelling system and laser innovation
- We plan to further extend our leadership with continued innovation in wafer stage and lens technology, also enabling extensions in our Application product portfolio
- Implementation of NXT platform for ArF together with the next generation stages



Next generation stage

Cost & uptime

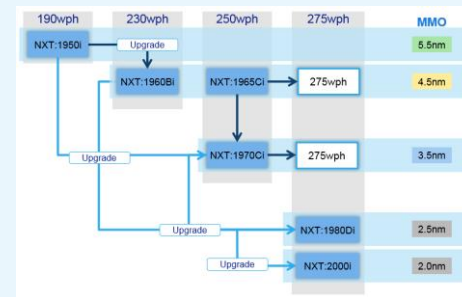
- NXT installed base has demonstrated >97% availability
- NXT:2000i already demonstrated 95% availability and ramped to mature reliability levels in 15 weeks, 2/3 the time required for the previous system NXT:1980i
- Leverage commonalities between models and platforms for cost efficiency and de-risking production



NXT:2000i reliability ramp-up

Installed Base Management

- Multiple opportunities to generate service revenue over the lifetime of a system
- Extended immersion upgrade path to NXT:2000i performance levels
- Strengthened our Installed Base Management product portfolio with value based service products



Extendibility upgrade paths

EUV: deliver performance for volume manufacturing and extend roadmap for continued cost effective shrink

3400B uptime improving to >90% for 2018/ 2019 HVM: Modular vessel acceleration

Acceleration improvements to <1.5nm overlay and 170wph

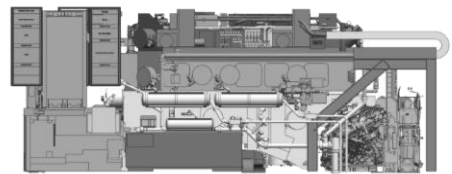
Extension to 3 nm node, through EXE5000 common subsystems, to <1nm overlay and >185wph

	2016	2017	2018	2019	2020	2021	2022	2023	...2025
EUV 0.33 NA 13nm	NXE:3350B 2.5 125wph	NXE:3400B 2.0nm 125wph	Overlay 1.5nm	TPut¹ 155	NXE:3400C 1.5nm 170wph		NXE Next 1.1nm ≥ 185wph		
0.55 NA 8nm								High NA 1.1nm 185wph	

Product
Matched Machine Overlay | Throughput



NXE:3400



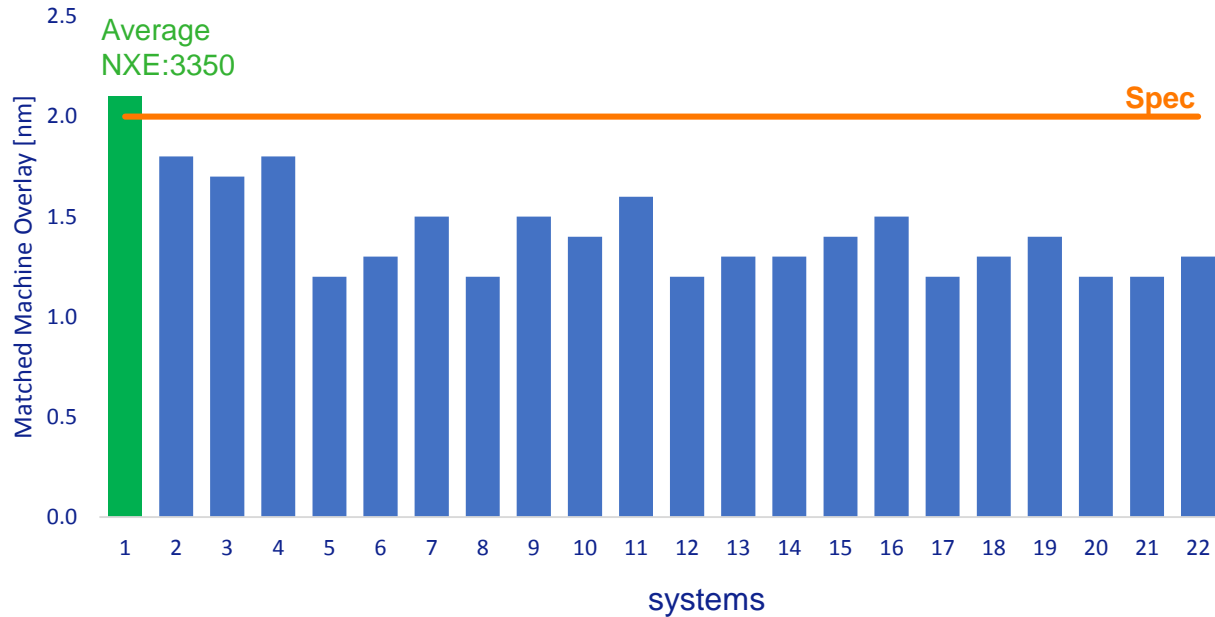
EXE:5000

High NA platform reducing need for multi-patterning 0.33 NA enabling long term litho simplification

¹ Tput: Throughput upgrade (wph)

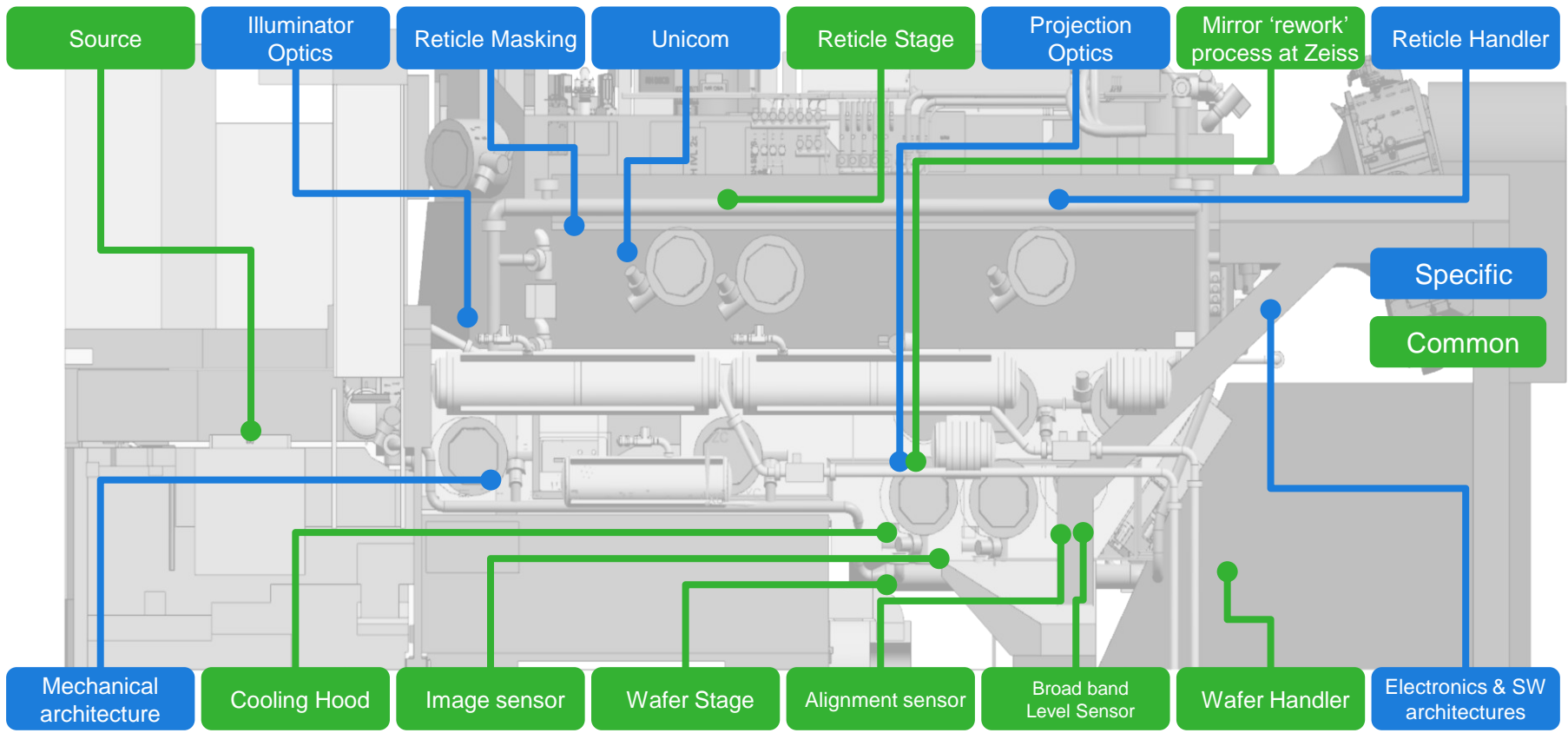
NXE:3400 Matched Machine Overlay

Performance well below NXE:3350 and specifications



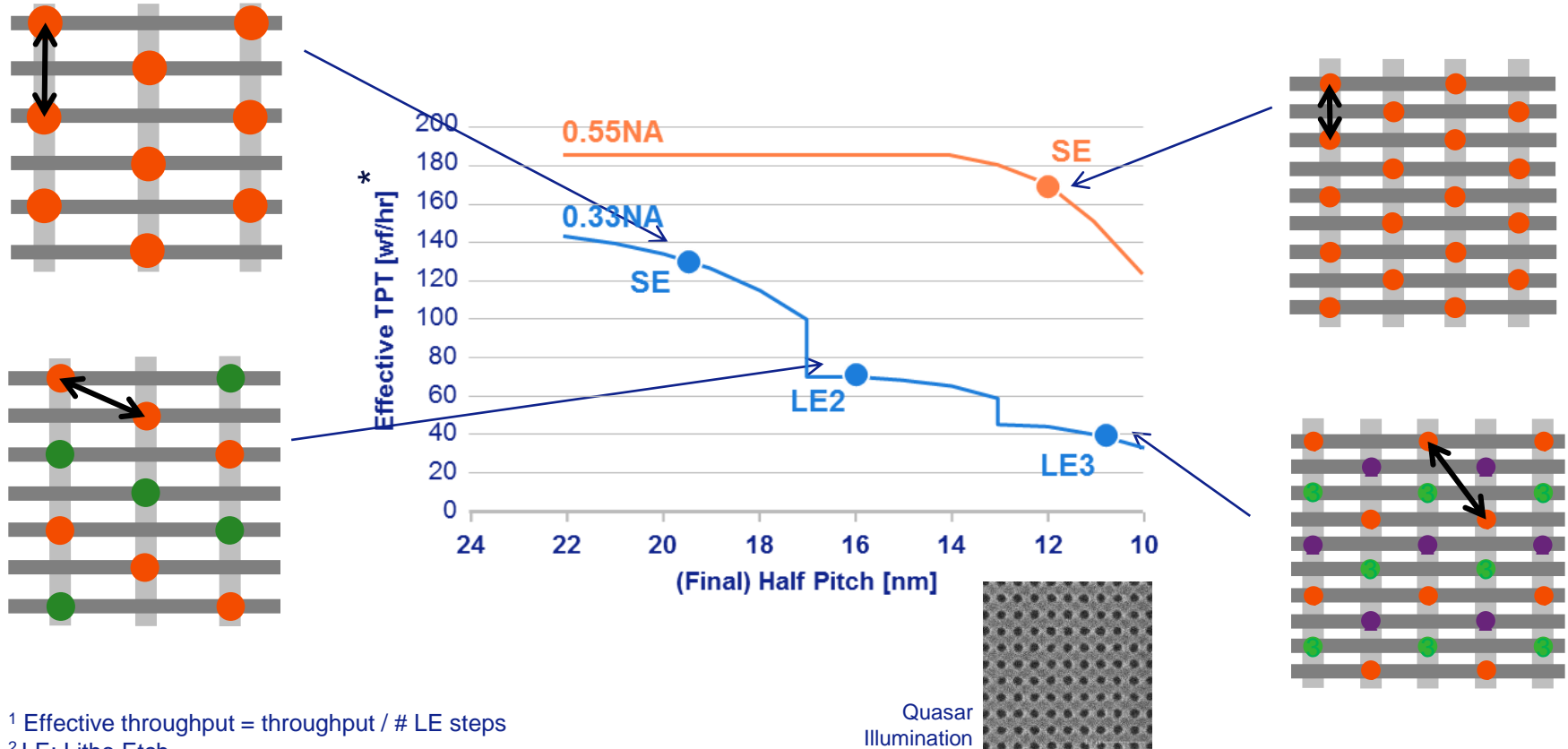
Driving commonality between High NA and 0.33 NA

Reduces risk, lowers cost and allow 0.33 extension



Larger NA results in higher effective throughput¹

Less number of Litho Etch² steps and transmission improvement



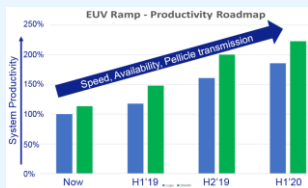
¹ Effective throughput = throughput / # LE steps

² LE: Litho Etch

EUV: two accelerated development programs in parallel after having achieved volume production feasibility metrics

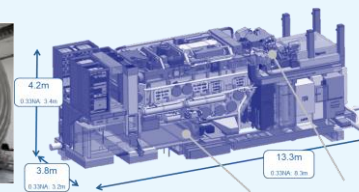
0.33 NA Summary

- ASML and supply chain preparing for planned production ramping
- Dedicated focus to improve availability across sites and systems
- Accelerated roadmap of NXE:3400C in order to deliver higher productivity tool, >170wph with improved availability
- Roadmap extended to the 3nm node working mix and match with DUV and High NA using common High NA and 0.33 NA innovations



High NA summary

- System design completed, module design progressing and key suppliers selected.
- Customers' roadmap aligned with the High NA introduction plan starting at 3nm.
- Three customers have committed to 4 R&D systems and 8 options for early volume systems. Results in total up to 1.5 B€ Customer commitments
- Design of metrology system by joint ASML-Zeiss team and manufacturing of optics started.
- Extended collaboration with imec in support of necessary developments in ecosystem and demo access for customers



Summary

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- Execution of our strategic priorities will provide required solutions for our customers, enabling cost effective shrink beyond the next decade

Forward Looking Statements

ASML

Public

Slide 26

8 November 2018

This document contains statements relating to certain projections, business trends and other matters that are forward-looking, including statements with respect to expected trends and outlook, strategy, bookings, expected financial results and trends, including expected sales, EUV revenue, gross margin, capital expenditures, R&D and SG&A expenses, cash conversion cycle, and target effective annualized tax rate, and expected financial results and trends for the rest of 2018 and 2019, expected revenue growth and demand for ASML's products in logic and memory, expected annual revenue opportunity in 2020 and for 2025 and expected EPS potential in 2020 with significant growth in 2025, expected trends in the lithography system market, fab capacity by segment, the automotive and artificial intelligence industries, connectivity, semiconductor end markets and new semiconductor nodes, expected acceleration of chipmakers' performance for the next decade, expected EUV insertion and transistor density growth, trends in DUV systems revenue and Holistic Lithography and installed based management revenues, statements with respect to expectations regarding future DUV sales, including composition, margins, improvement of operations and performance, DUV product roadmaps, expected benefits of the holistic productivity approach, including in terms of wafers per year, expected industry trends and expected trends in the business environment, statements with respect to customer demand and the commitment of customers to High NA machines and to insert EUV into volume manufacturing by ordering systems, expected future operation of the High NA joint lab, statements with respect to holistic lithography roadmaps and roadmap acceleration, including the introduction of higher productivity systems in 2019 (including the expected shipment of NXE:3400C and expected timing thereof) and the expected benefits, ASML's commitment to volume manufacturing and related expected plans until 2030, ASML's commitment to secure system performance, shipments, and support for volume manufacturing, including availability, timing of and progress supporting EUV ramp and improving consistency, productivity, throughput, and production and service capability enabling required volume as planned, including expected shipments, statements with respect to growth of fab capacity driving demand in lithography systems, planned customer fabs for 200 systems and expected first output in 2019, expected EUV value increase and increase in EUV margins and ASML's expectation of EUV profitability at the DUV level, expected installed base of EUV systems, expected customer buildout of capacity for EUV systems, EUV estimated demand by market, expected increase in lithography intensity, statements with respect to the expected benefits of EUV, including year-on-year cost reduction and system performance, and of the introduction of the new DUV system and expected demand for such system, the expected benefits of HMI's e-beam metrology capabilities, including the expansion of ASML's integrated Holistic Lithography solutions through the introduction of a new class of pattern fidelity control, the extension of EUV to enable cost effective single patterning shrink with EUV, statements with respect to ASML's applications business, including statements with respect to expected results in 2018, expected growth of the applications business and expected drivers of growth, expected growth in margins, continued shrink and drivers, and expected accuracy, defect control and performance improvements, shrink being a key driver supporting innovation and providing long-term industry growth, lithography enabling affordable shrink and delivering value to customers, DUV, Holistic Lithography and EUV providing unique value drivers for ASML and its customers, expected industry innovation, the expected continuation of Moore's law and that EUV will continue to enable Moore's law and drive long term value for ASML beyond the next decade, intention to return excess cash to shareholders through stable or growing dividends and regularly timed share buybacks in line with ASML's policy, statements with respect to the expectation to continue to return cash to shareholders through dividends and share buybacks, and statements with respect to the expected impact of accounting standards. You can generally identify these statements by the use of words like "may", "will", "could", "should", "project", "believe", "anticipate", "expect", "plan", "estimate", "forecast", "potential", "intend", "continue", "targets", "commits to secure" and variations of these words or comparable words. These statements are not historical facts, but rather are based on current expectations, estimates, assumptions and projections about the business and our future financial results and readers should not place undue reliance on them.

Forward-looking statements do not guarantee future performance and involve risks and uncertainties. These risks and uncertainties include, without limitation, economic conditions, product demand and semiconductor equipment industry capacity, worldwide demand and manufacturing capacity utilization for semiconductors, including the impact of general economic conditions on consumer confidence and demand for our customers' products, competitive products and pricing, the impact of any manufacturing efficiencies and capacity constraints, performance of our systems, the continuing success of technology advances and the related pace of new product development and customer acceptance of and demand for new products including EUV and DUV, the number and timing of EUV and DUV systems shipped and recognized in revenue, timing of EUV orders and the risk of order cancellation or push out, EUV production capacity, delays in EUV systems production and development and volume production by customers, including meeting development requirements for volume production, demand for EUV systems being sufficient to result in utilization of EUV facilities in which ASML has made significant investments, potential inability to successfully integrate acquired businesses to create value for our customers, our ability to enforce patents and protect intellectual property rights, the outcome of intellectual property litigation, availability of raw materials, critical manufacturing equipment and qualified employees, trade environment, changes in exchange rates, changes in tax rates, available cash and liquidity, our ability to refinance our indebtedness, distributable reserves for dividend payments and share repurchases, results of the share repurchase plan and other risks indicated in the risk factors included in ASML's Annual Report on Form 20-F and other filings with the US Securities and Exchange Commission. These forward-looking statements are made only as of the date of this document. We do not undertake to update or revise the forward-looking statements, whether as a result of new information, future events or otherwise.

Public

ASML

INVESTOR DAY

ASML **SMALL** **TALK** **2018**

VELDHOVEN

