Technology Strategy to Drive Moore's Law into Next Decade
Martin van den Brink
President and
Chief Technology Officer
Public
ASML
ASML
Small
Talk
2021
Investor Day
Virtual

Technology strategy
Key messages

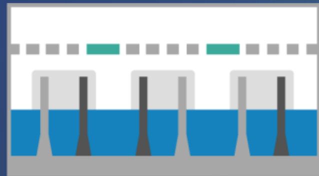
- **Moore's Law is alive and well!** Industry innovation continues, fueled by system scaling, delivering highly valued semiconductor products.
- **Semiconductor system scaling** enables exponential performance improvement and energy reduction in support of significant growth of data exchange.
- **Customers' roadmaps** require continued shrink and reduction in edge placement error to drive affordable scaling into next decade.
- **Holistic Lithography roadmap** is driven by our unique patterning control solutions that deliver customer value via improved on product performance.
- **ASML's comprehensive product portfolio** is aligned to our customers' roadmaps, delivering cost effective solutions in support of all applications from leading edge to mature nodes
- **Our next generation EUV technology, High-NA,** is progressing well and will be the engine to drive the lithography roadmap into the next decade
- **Continued execution of our strategic priorities** is expected to provide cost effective solutions for our customers, enable the extension of the industry roadmap into the next decade, and support our long-term sustainability commitment

- **Moore's Law evolution and customer roadmap**

ASML's strategic priorities

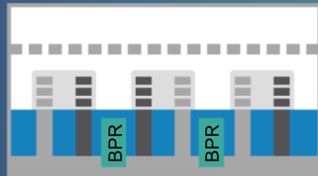
Significant device innovation in logic ahead of us

scaling roadmap continues to 1 nm and beyond



FinFET

5T

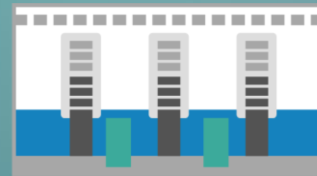


Nanosheets, BPR

5T

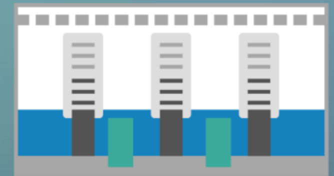
Forksheets, VHV std cell arch.

<5T



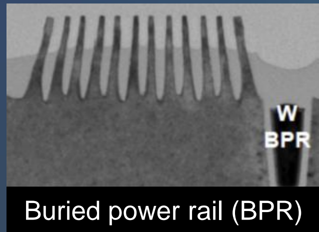
CFET, BEOL w/airgaps

4T

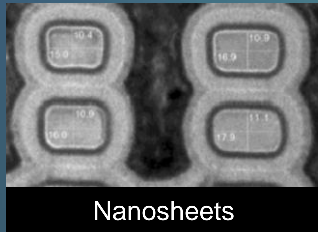


2D atomic channels

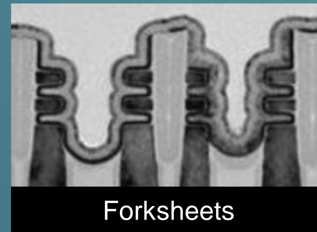
<4T



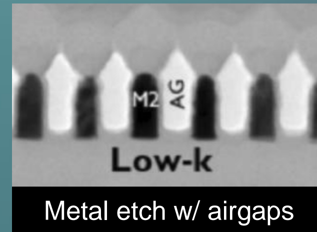
Buried power rail (BPR)



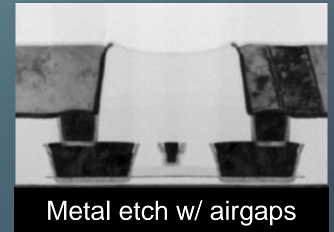
Nanosheets



Forksheets



Metal etch w/ airgaps



Metal etch w/ airgaps

VHV: Vertical-Horizontal-Vertical

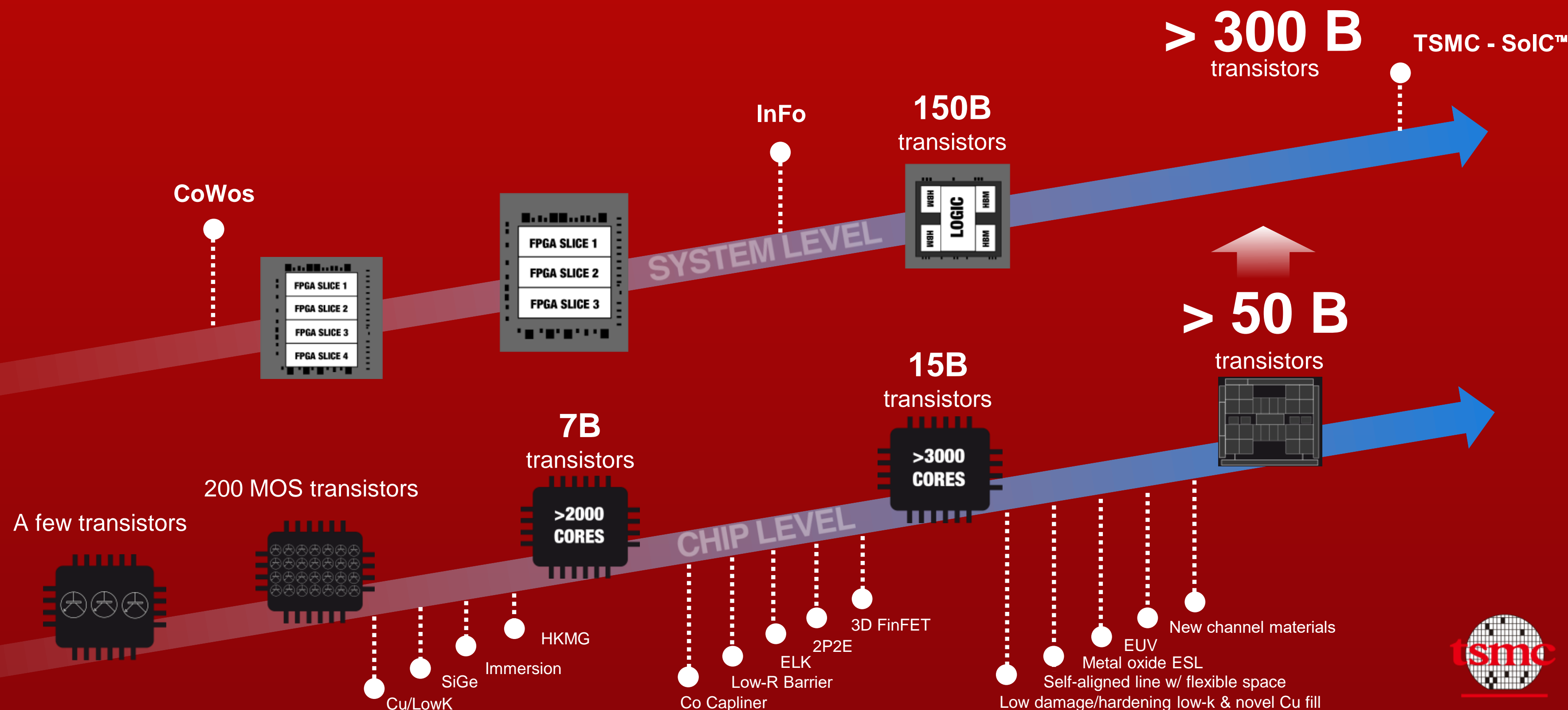
PP: Poly Pitch (nm)
MP: dense metal pitch (nm)
CFET: Complementary FET

Source: IMEC, Sri Samavedam, “Future logic scaling: Towards atomic channels and deconstructed chips”, IEDM, December 2020.

Innovation is not limited to device level

TSMC's system roadmap to >300 B transistors

SOC: System on Chip
WoW: Wafer on Wafer
CoW: Chip on Wafer
CoWoS: Chip on Wafer on Substrate
FPGA: Field Programmable Grid Array
HBM: 3D High Speed Memory
InFo: Integrated Fan-Out
RDL: Re Distribution Layer
SoIC: System on Integrated Chips

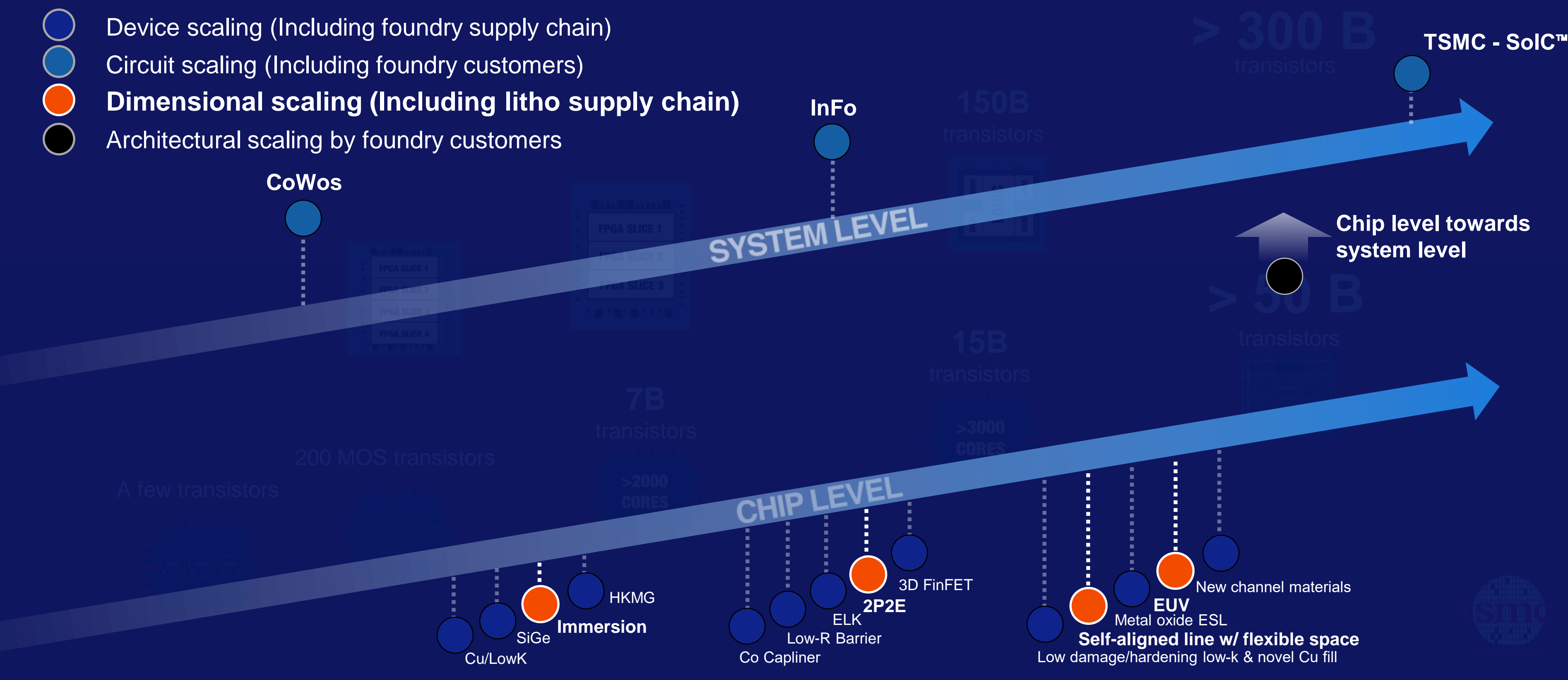


Source: Mark Liu, TSMC, "Unleash the future of innovation" ISSCC, Feb 15, 2021

Innovation is not limited to device level

TSMC's system roadmap to >300 B transistors

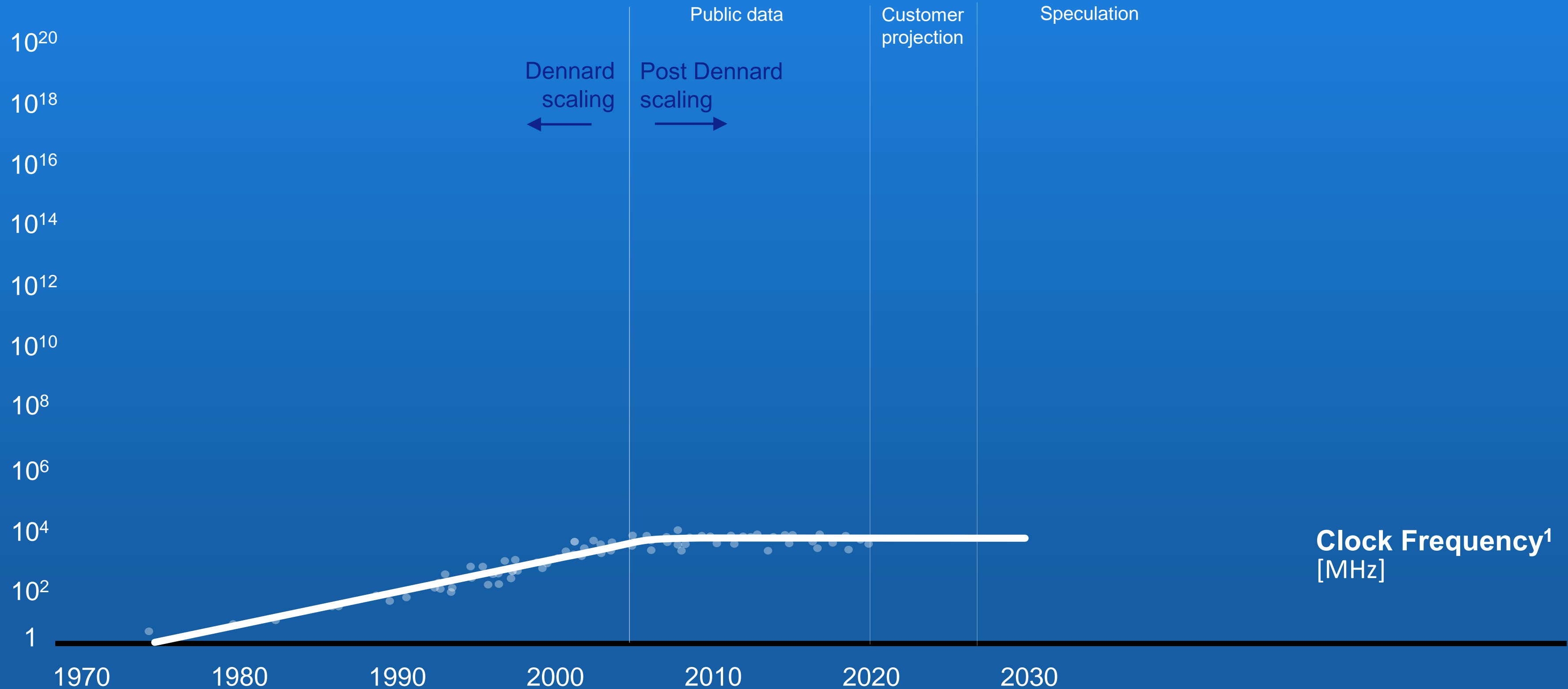
SOC: System on Chip
WoW: Wafer on Wafer
CoW: Chip on Wafer
CoWoS: Chip on Wafer on Substrate
FPGA: Field Programmable Grid Array
HBM: 3D High Speed Memory
InFo: Integrated Fan-Out
RDL: Re Distribution Layer
SoIC: System on Integrated Chips



Source: Mark Liu, TSMC, "Unleash the future of innovation" ISSCC, Feb 15, 2021

Moore's Law evolution: the next decade

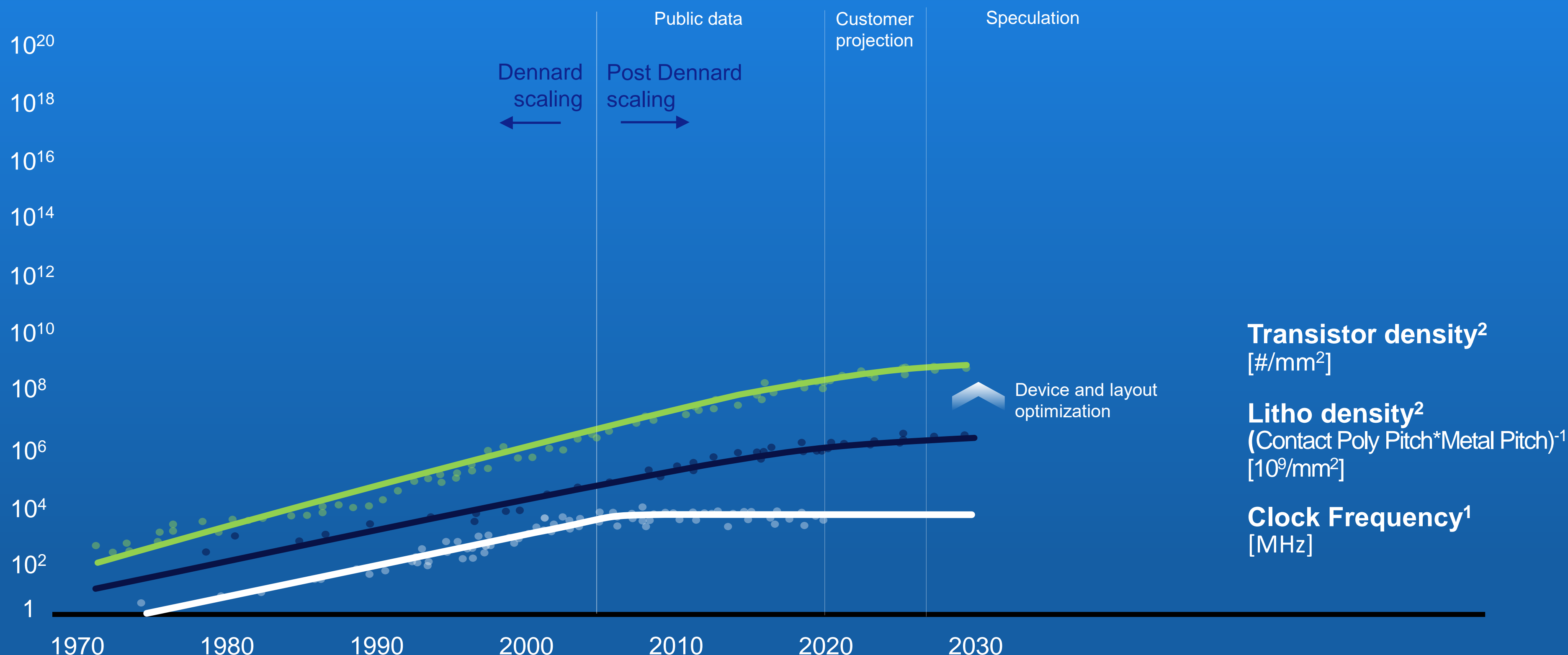
Traditional scaling metrics like clock frequency have been saturated since 2005



Source: [1]Karl Rupp as published by: Shekar Bokar, QUALCOMM, "Future of computing in the so-called post Moore's Law era", International conference for high performance computing, networking storage and analysis, November 18, 2020.

Moore’s Law evolution: the next decade

Scaling metric of transistor and litho density continues in this decade



Sources: [1]Karl Rupp [2]ASML data and projection using Rupp

Moore’s Law evolution: the next decade

A system metric measuring energy and time efficiency combined

- Energy-Efficient Performance for systems and devices defined as

$$EEP = \frac{\text{\# of operations per sec.}}{\text{energy per operation}} \quad [1/J \cdot s]$$

- If applied per single device:

$$EEP = f_c/e$$

f_c = clock frequency [s^{-1}]

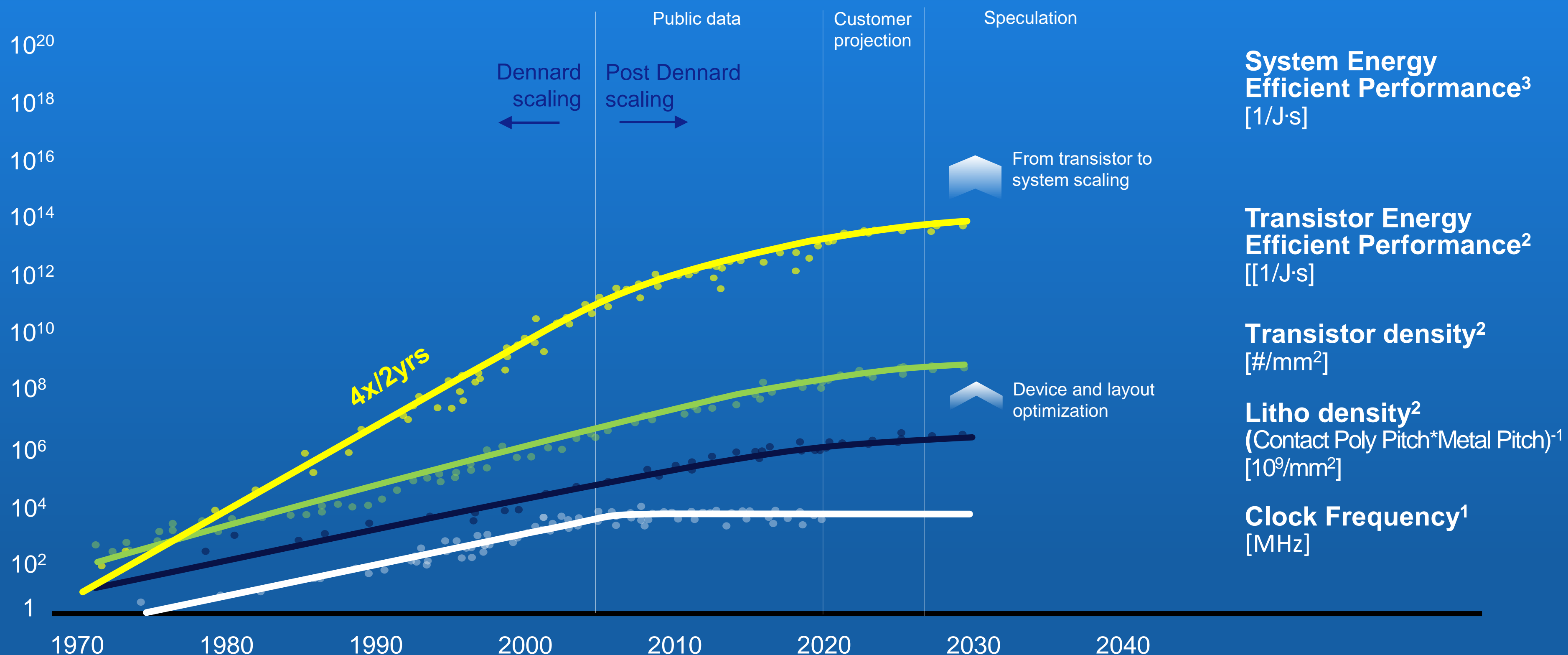
e = the transistor switch energy [J]

- Using the Dennard[1] scaling model, when the dimension scales with k^{-1}, frequency with k, area with k^{-2} and power density constant, it follows:
    - EEP on-device level scales with k^4
- If density ($\sim k^2$) scales 2x every 2 year, then EEP ($\sim k^4$) scales 4x every 2 year

[1]Source: Robert H. Dennard et al. “Design of ion implanted MOSFET’s with very small physical dimensions”, IEEE Journal of solid-state circuits, vol SC 9, October 1973, pp. 256-268.

Moore's law evolution: the next decade

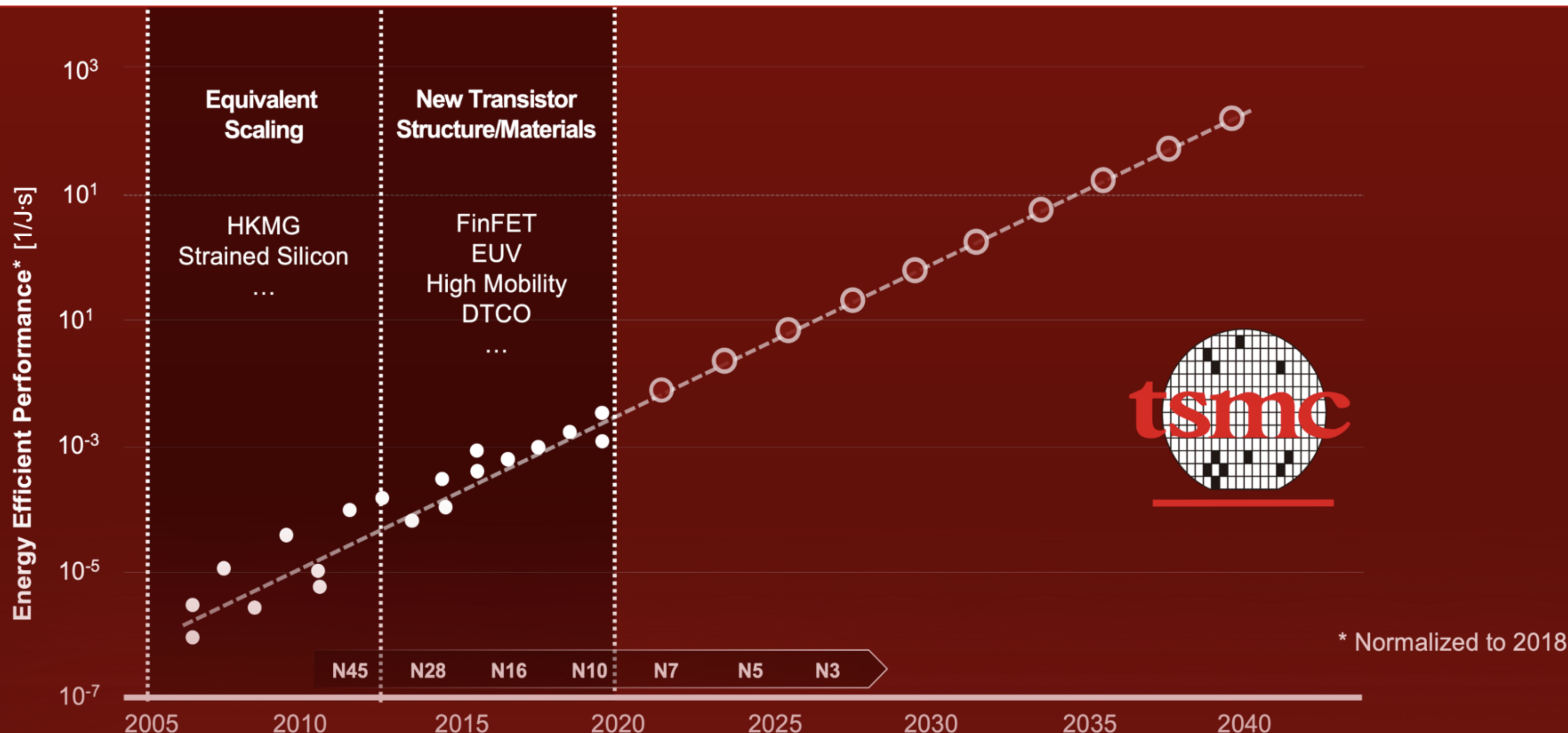
Device Energy Efficient Performance growth been saturated since 2005



Sources: [1]Karl Rupp, [2] ASML data and projection using Rupp

Moore's Law evolution: the next decade

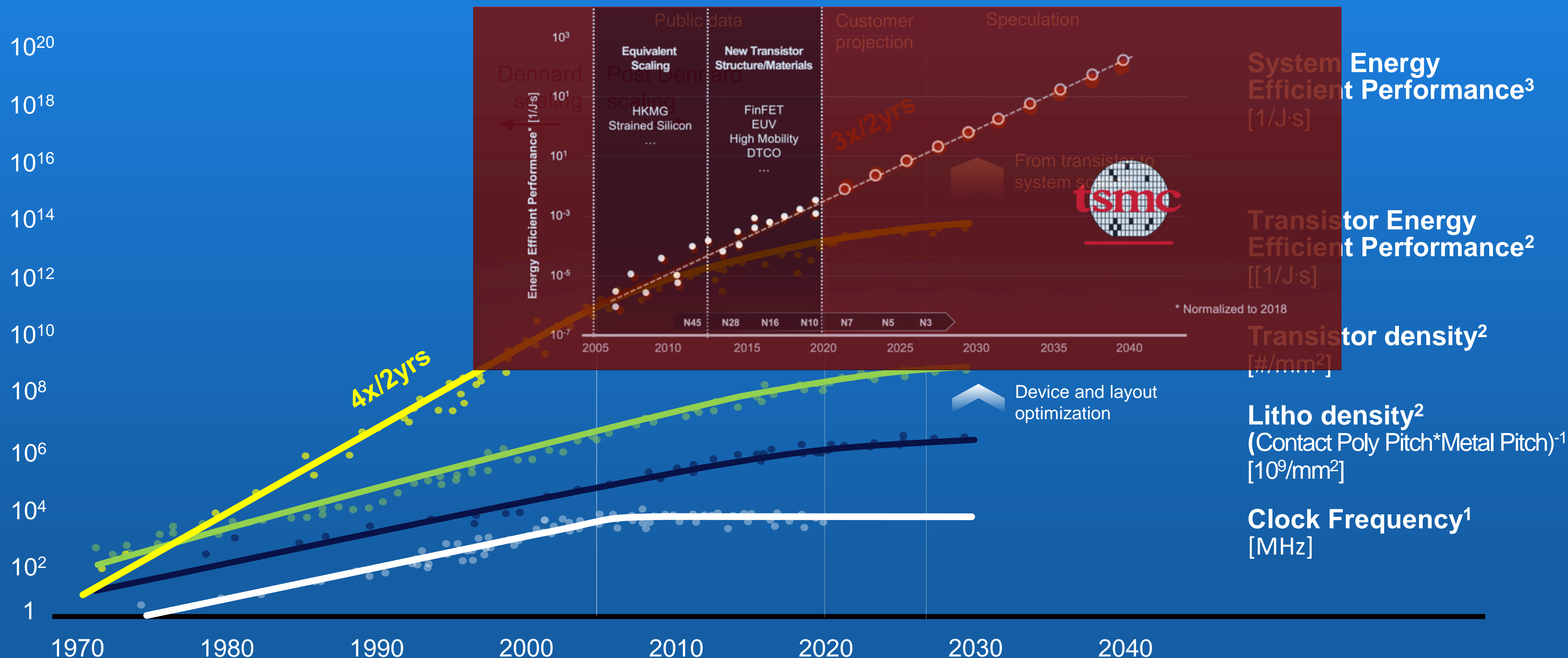
System Energy Efficient Performance growth 3x/2yrs continues to 2040



Source: TSMC, Mark Liu, "Unleash the future of innovation" ISSCC, Feb 15, 2021.

Moore’s law evolution: the next decade

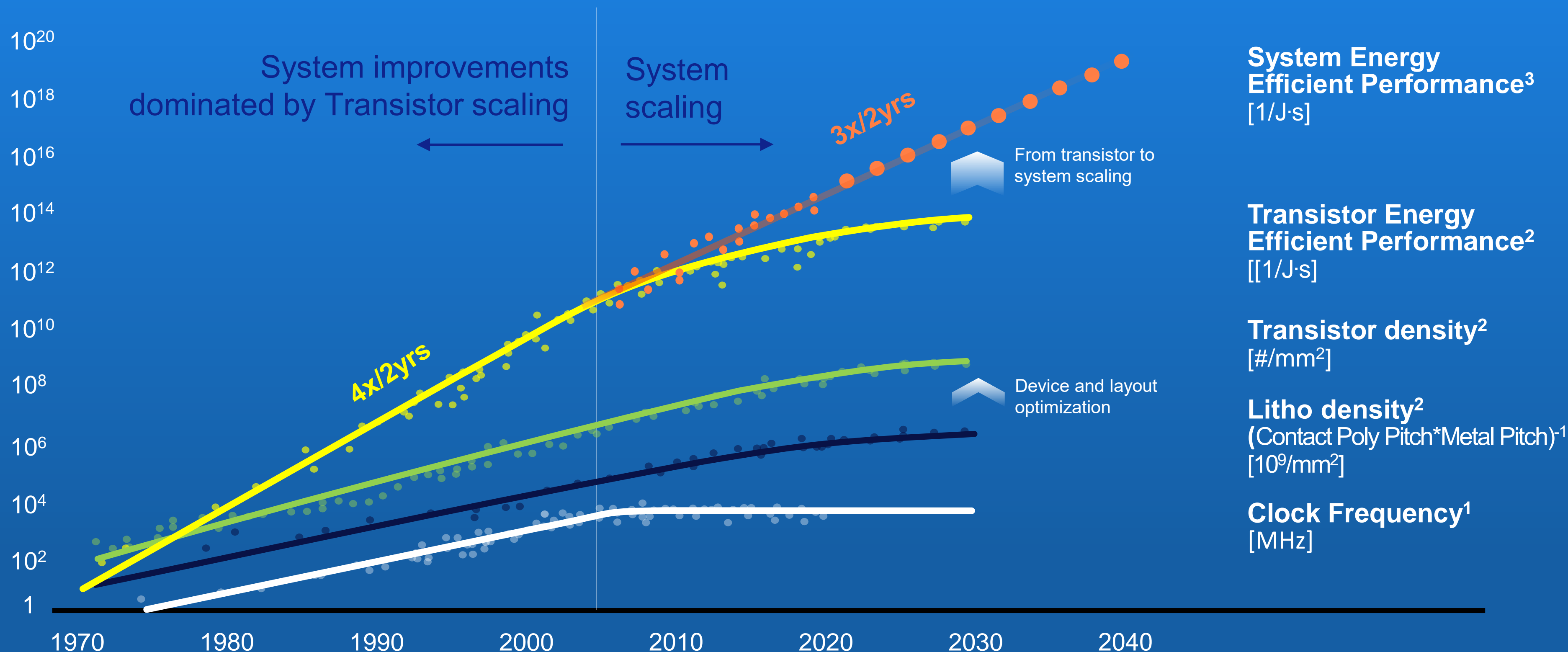
From cost per transistor through density, to cost of time and energy through systems



Sources: [1]Karl Rupp, [2]ASML data and projection using Rupp, [3]Mark Liu, TSMC, normalized to transistor EEP in 2005.

Moore's law evolution: the next decade

System scaling to satisfy the need for performance and energy consumption

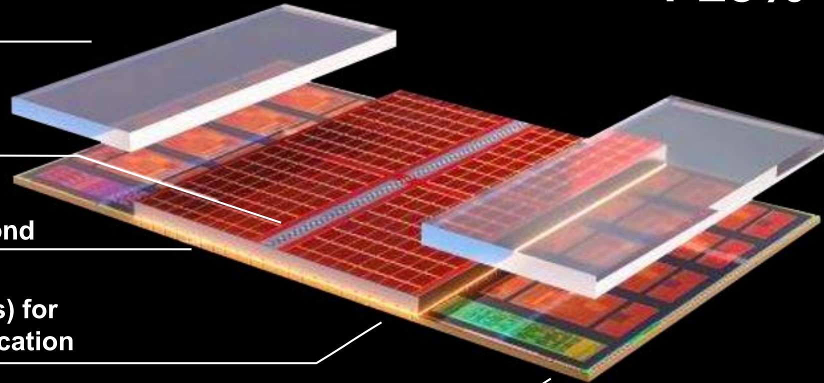


Sources: [1]Karl Rupp, [2]ASML data and projection using Rupp, [3]Mark Liu, TSMC, normalized to transistor EEP in 2005.

AMD 3D chiplet gives an 3.1-3.8 EEP improvement

By integrating memory with the processor in one package

**3x power reduction,
4-25% speed improvement**



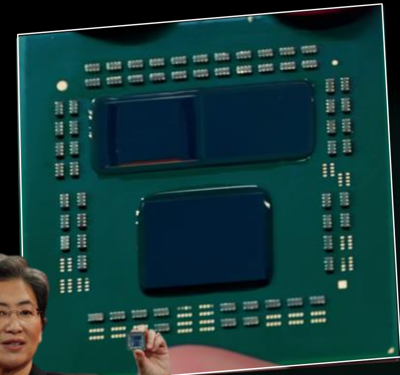
Structural silicon

64MB L3 cache die

Direct copper-to-copper bond

Through Silicon Vias (TSVs) for silicon-to-silicon communication

Up to 8-core "Zen 3" CCD



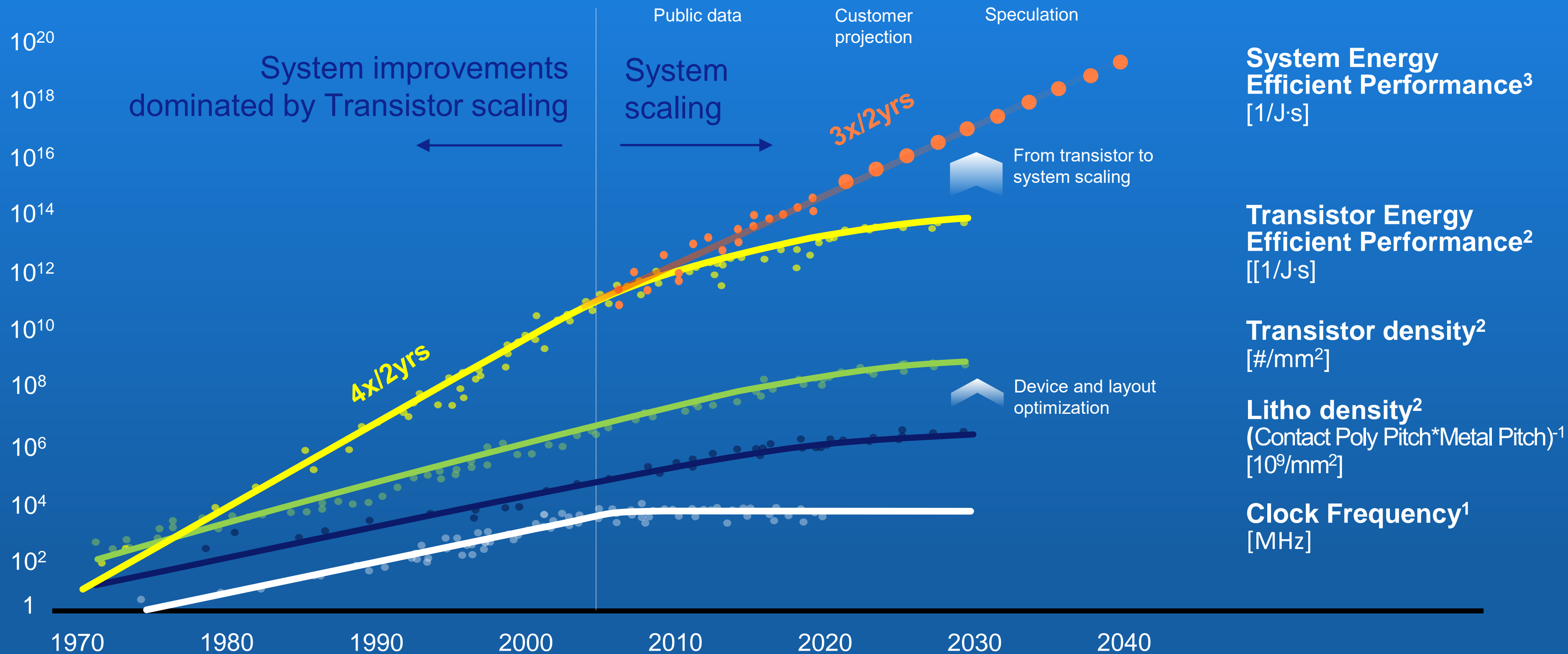
Source: Lisa Su, AMD,
"Accelerating the ecosystem", Computex keynote 2021, June 2 2021

AMD

Moore's law evolution: the next decade

System scaling to satisfy the need for performance and energy consumption

Slide 15
29 Sept. 2021

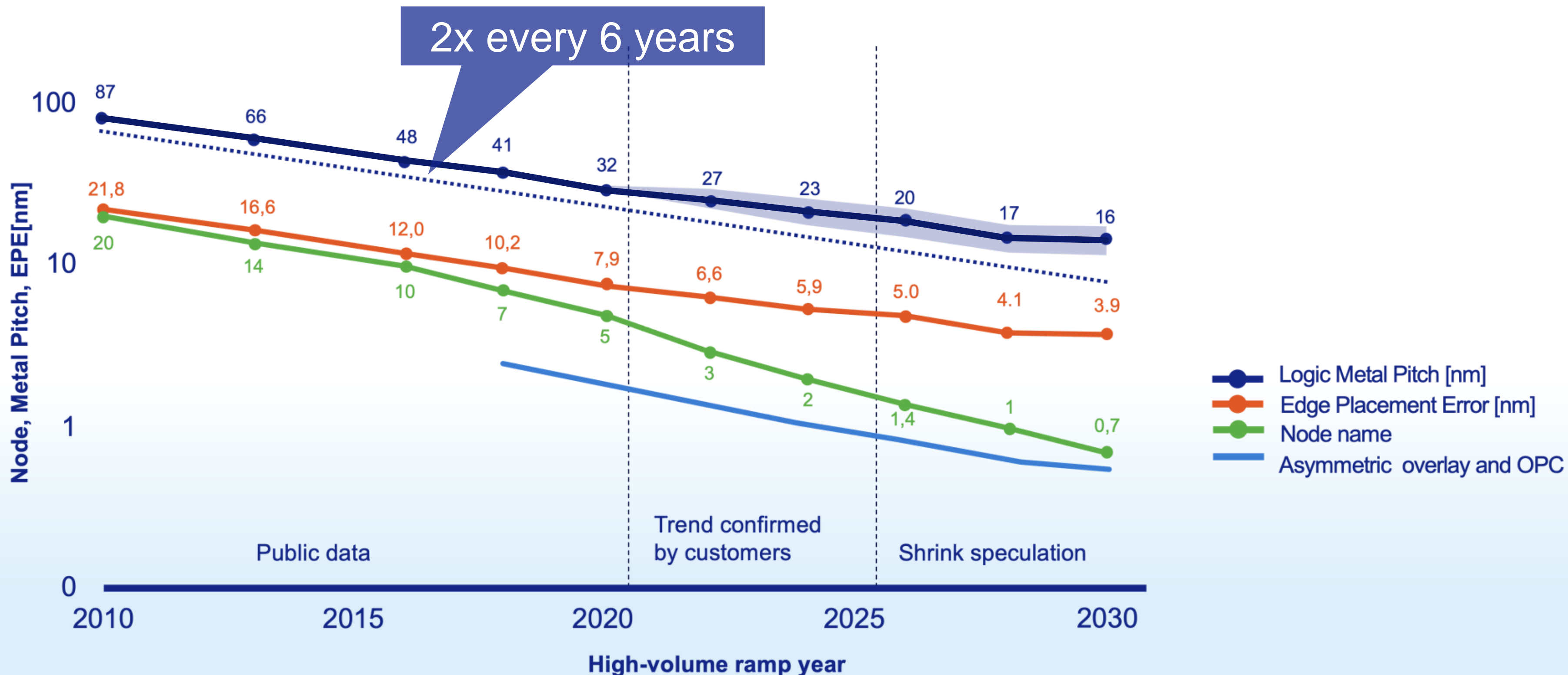


Sources: [1]Karl Rupp, [2]ASML data and projection using Rupp, [3]Mark Liu, TSMC, normalized to transistor EEP in 2005.

Public

Litho density scaling continues in this decade

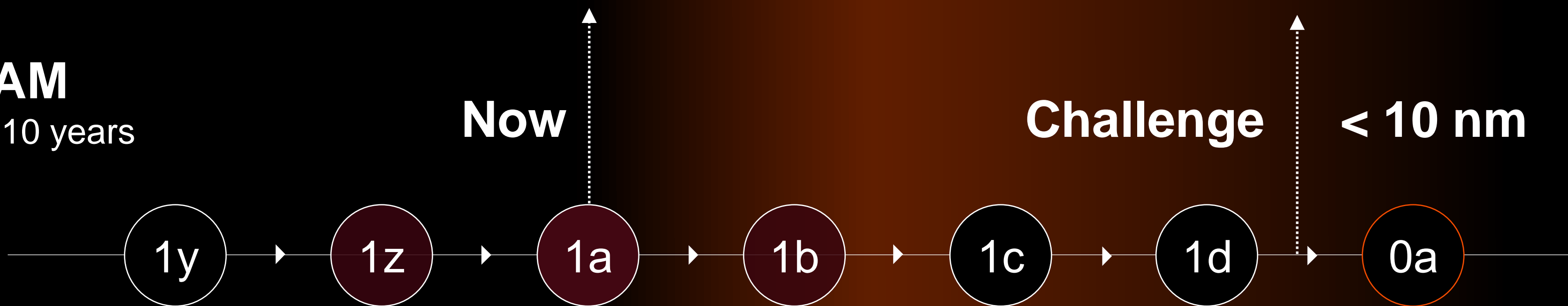
Overlay and Optical Proximity Correction errors shrink aggressively

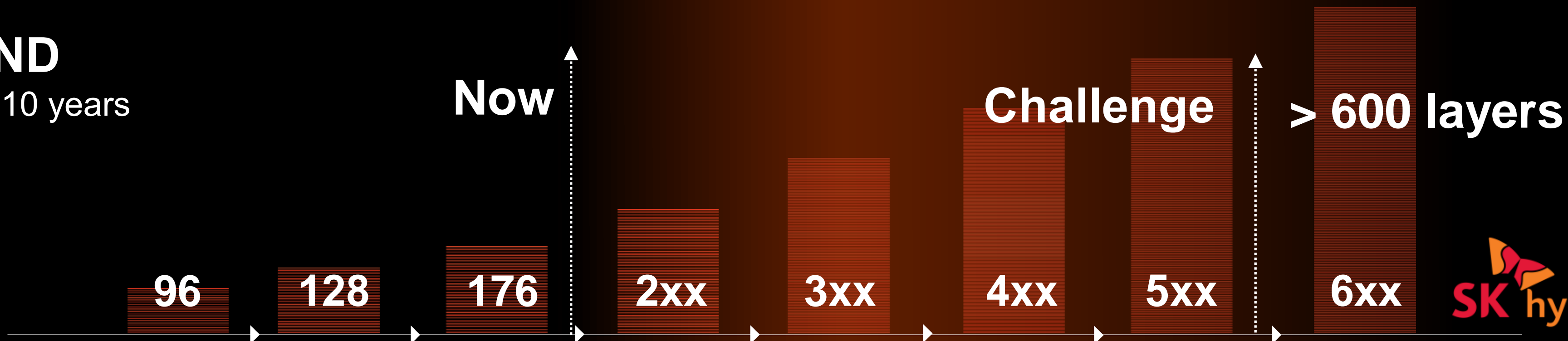


Source: Average customer roadmap extended by ASML extrapolation May 2021, averaged with 2020 IRDS Roadmap Mustafa Badaroglu, “IRDS IFT – More Moore Spring meeting, IEEE, April 21, 2020

Memory roadmap for the next decade

DRAM scaling below 10 nm and NAND stacking continues > 600 layers



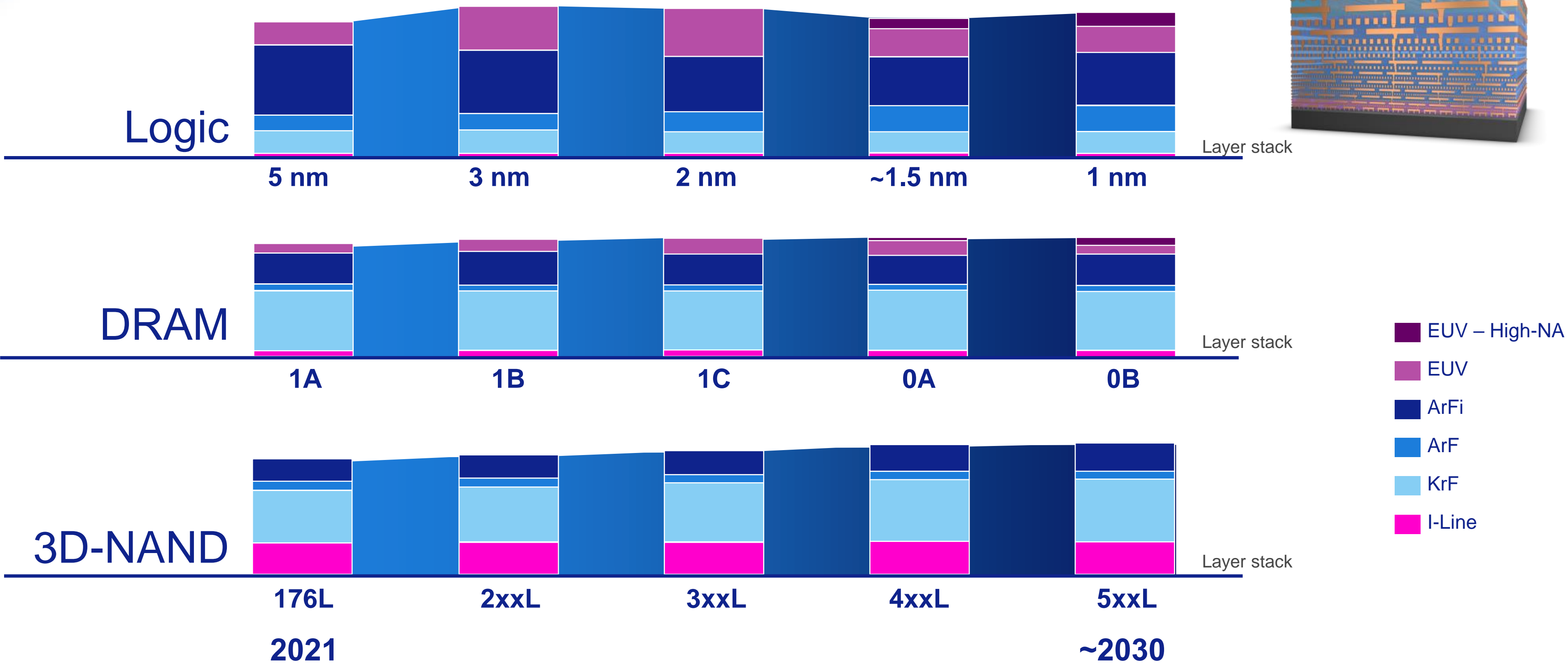


Source: Sk hynix, S.H.Lee, "Memory's journey towards the future ITC world, IEEE IRPS 21 March 21, 2021

Projection of lithography layers by technology

ASML

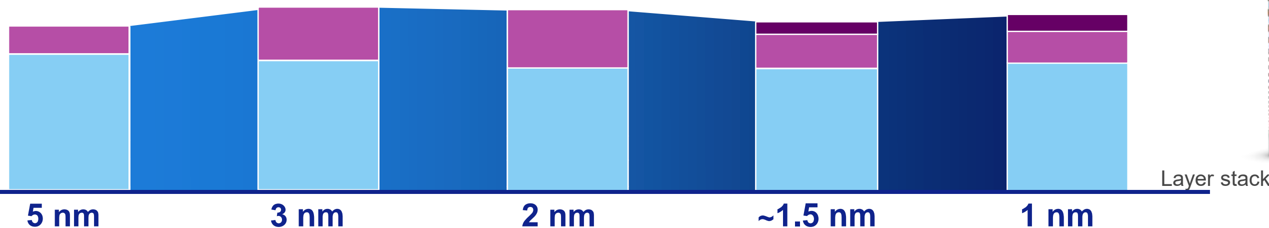
Slide 18
29 Sept. 2021

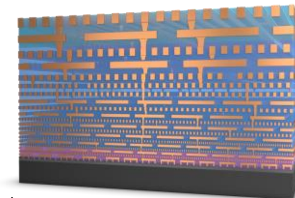


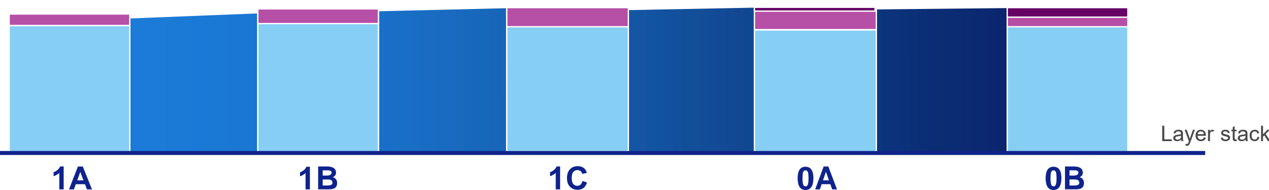
Source: ASML Corporate Strategy and Marketing estimates

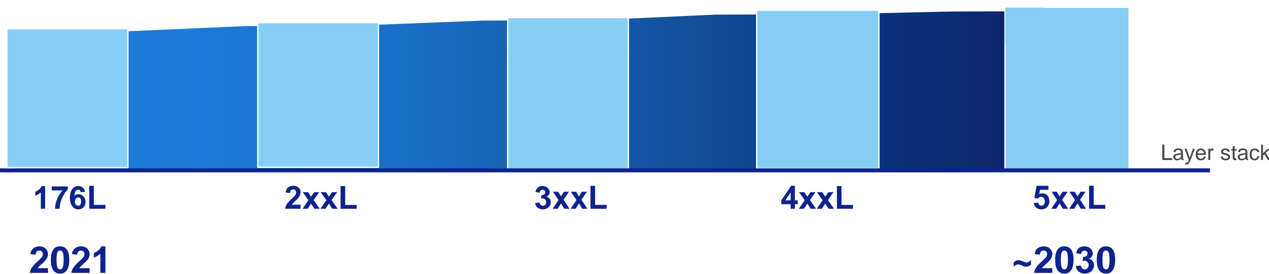
Projection of lithography layers by technology

Lithography layer count grows, driven by DUV and EUV



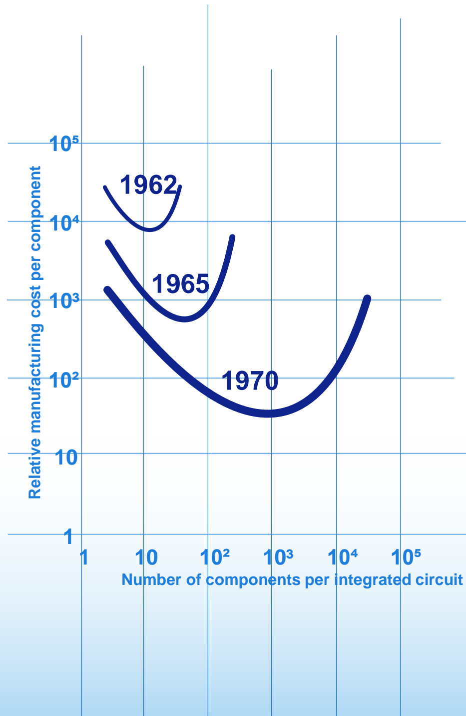






Source: ASML Corporate Strategy and Marketing estimates

Semiconductor and shrink roadmap: the next decades



In the next decade, system scaling continues to fuel the need of advanced semiconductor solutions where litho shrink remains key to improving circuit density and cost.

Implications for ASML

The shrink roadmap requires innovation to improve litho performance at lower cost and higher productivity.

We continue to safeguard our approach by developing **trusting relationships with customers, with stronger holistic products.**

Moore's Law evolution and customer roadmap

- **ASML's strategic priorities**

ASML's strategic priorities

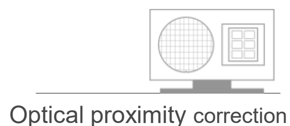
Priority	
Strengthen customer trust	▪ Enhance execution capabilities to deliver performance, cost and robustness to customers needs
Holistic litho and applications	▪ Build a leading position in edge placement error
DUV competitiveness	▪ Drive DUV performance and market share
EUV industrialization	▪ EUV high-volume production performance, ramp and support
High-NA	▪ Enable litho simplification for future nodes

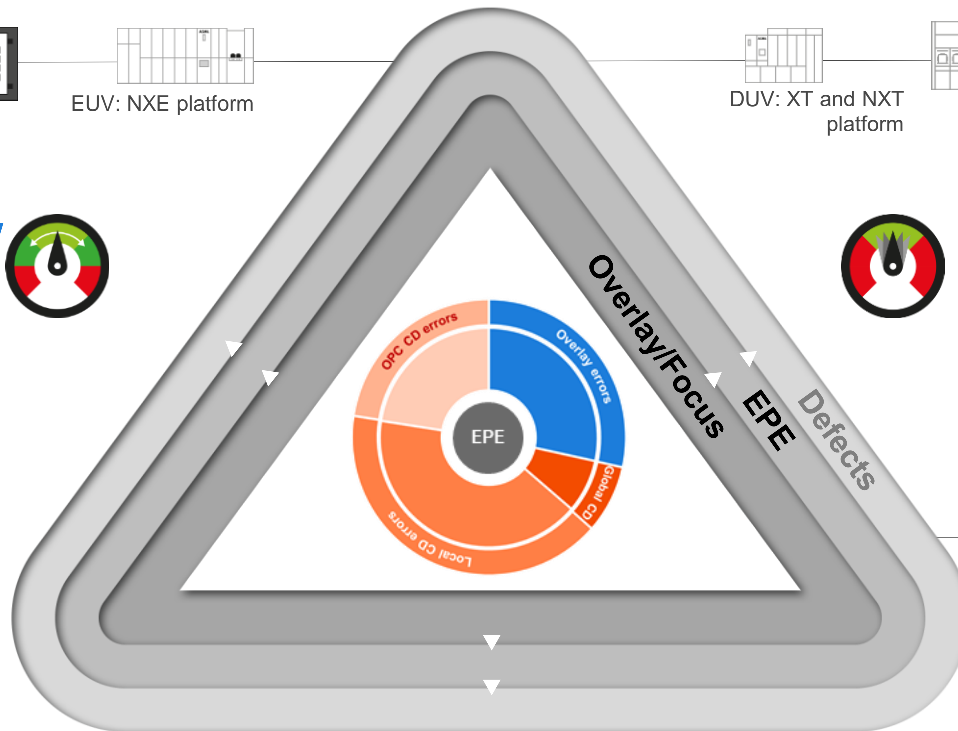
Our holistic portfolio is more important than ever

Lithography scanner with advanced control capability

Process window
Prediction and Enhancement

Process window
Control



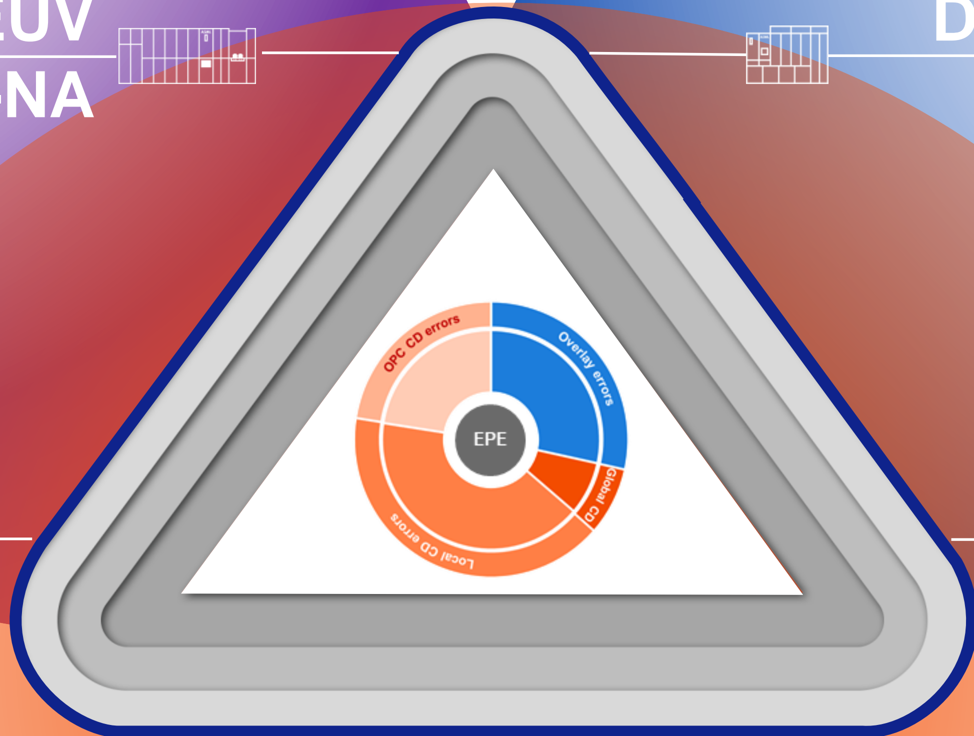


Computational lithography and computational metrology

Optical metrology
E-beam metrology
E-beam inspection

Process window
Detection

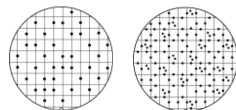
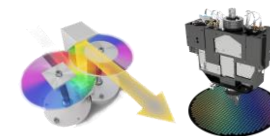
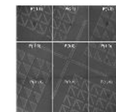
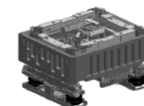
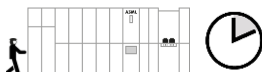
Our holistic portfolio is more important than ever



APPS

Applications: strategic directions

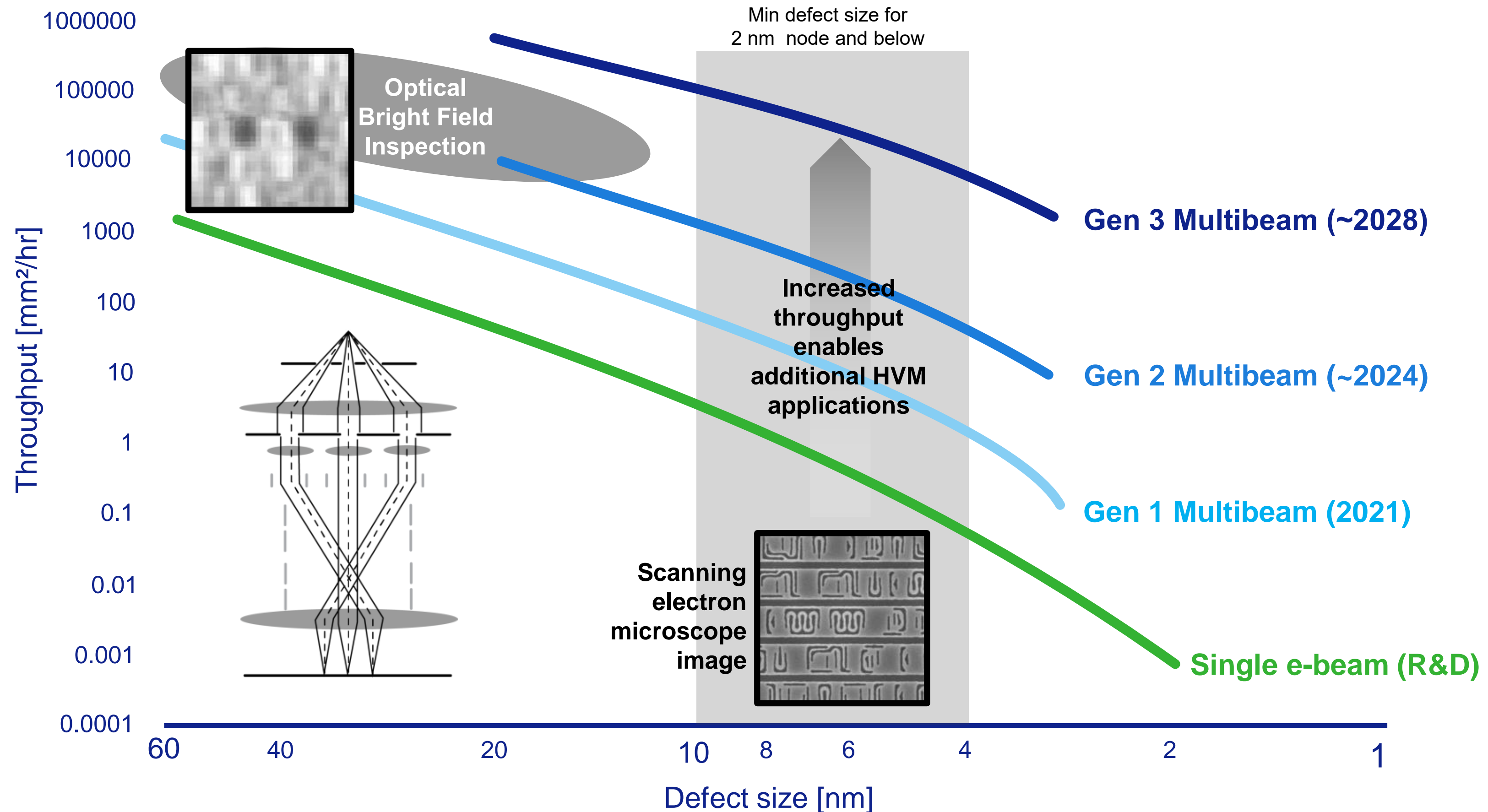
Deliver leading solutions for optical and e-beam metrology and inspection

	Customer Value	ASML Apps product roadmap	
 **Nanometers**	Capturing more wafer signatures to improve robust on-wafer process control	• Productivity • Robust alignment schemes	
Good wafers per day per unit cost	Tighter process capabilities 3→6 sigma control	• Single Beam resolution and applications • Edge Placement Error control • Free-Form OPC and Machine Learning	
	Capturing small defects for yield of advanced nodes	• Multibeam resolution • Computationally guided inspection	
	More measurements at fixed metrology & inspection budget	• Productivity/multibeam • E-beam platform consolidation	
 **Time to yield**	Faster time-to-solution	• OPC accuracy, speed and user-friendliness • Single process control platform and analytics	

E-beam inspection has inherent resolution advantage

Increasing throughput through increasing parallelism with multibeam

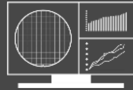
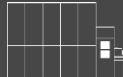
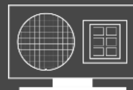
ASML



APPS

Metrology, Inspection & Patterning Control Roadmap

ASML

	2020 | 2021 | 2022 | 2023 | 2024 | ≥ 2025
Scanner Interfaces and Control Software 	Increasing Scanner Actuation (DUV and EUV), EPE Control
Overlay Metrology YieldStar	Fast Stages, Multiple Wavelengths, Computational Metrology, In-Device Metrology
E-beam Metrology	Single Beam High Resolution, Large Field of View, Massive Metrology, EPE metrology
E-Beam Defect Inspection 	Multi-beam, Fast and Accurate Stages, High Landing Energy, Guided Inspection
Computational Lithography 	Improved Model Accuracy, Inverse OPC, Machine and Deep Learning, Etch Models

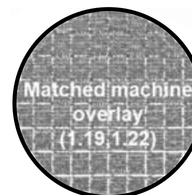
DUV

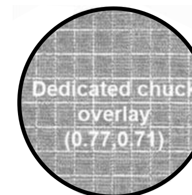
NXT:2050i in volume manufacturing at customers

20% overlay improvement, faster reliability and productivity ramp-up

ASML

NXT:2050i

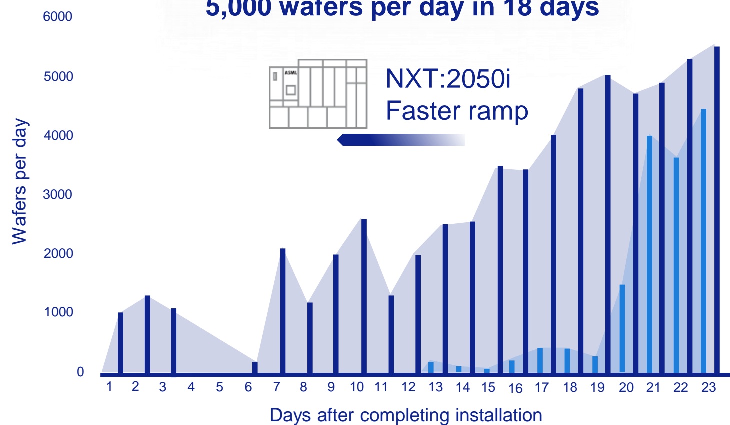




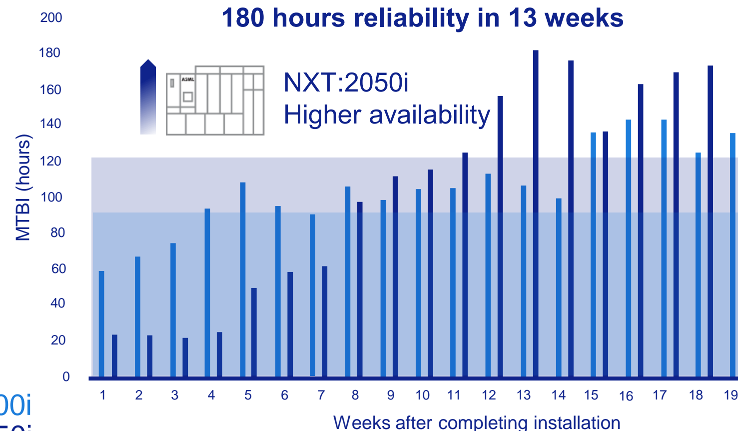
Matched machine overlay ~1.2 nm

Dedicated chuck overlay ~0.8 nm

5,000 wafers per day in 18 days



180 hours reliability in 13 weeks



NXT:2000i
NXT:2050i

DUV

DUV: Strategic directions

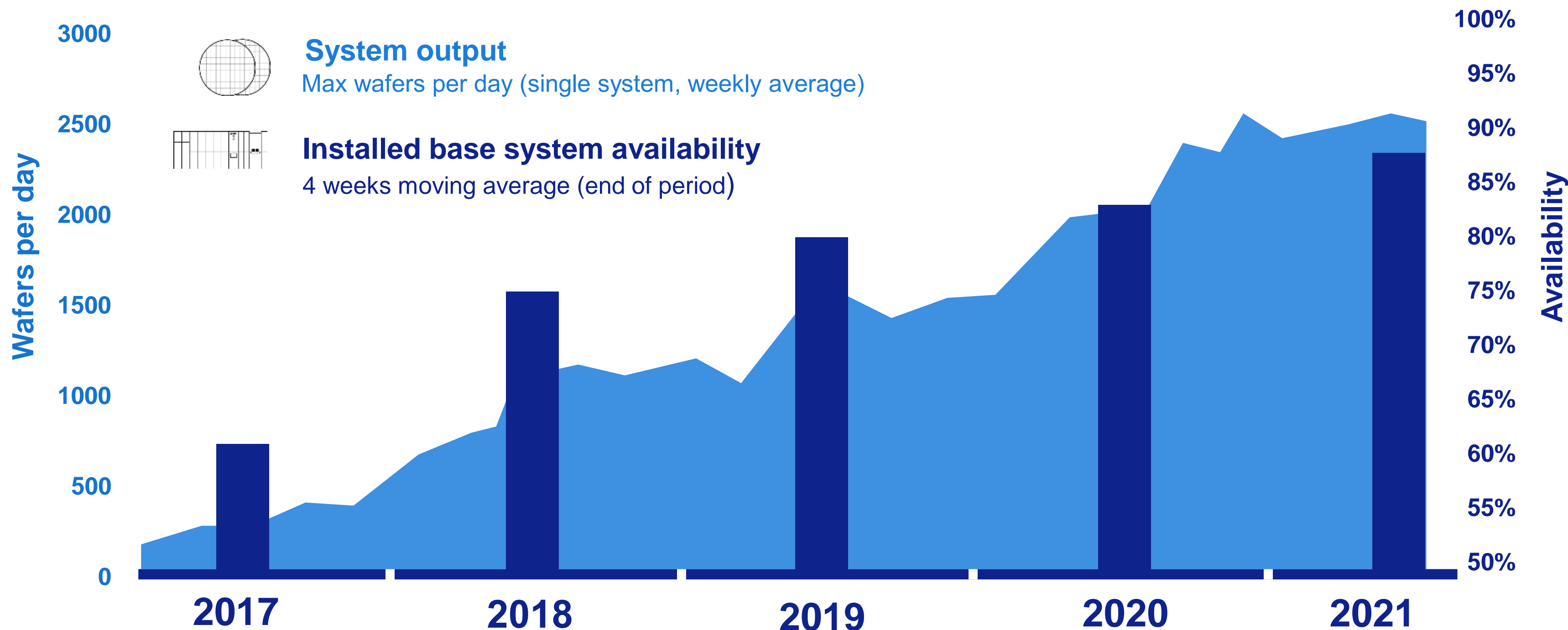
Deliver leading solutions for advanced capabilities and higher productivity

	Customer value	ASML DUV product roadmap
Overlay	Improve overlay (stability) especially for matching to EUV	• NXT:2100i with optics and alignment improvements
Productivity & Availability	More good wafers per day at lower cost per wafer	• Immersion productivity increase through higher scan speed • XT to NXT transition for dry lithography
Installed base	Cost-competitive service offerings for entire product lifecycle	• Productivity Enhancement Packages for installed base • Value added service solutions increasing availability at node performance
New markets	Productivity and overlay performance for specific applications	• Mature XT platform with application specific options • Extend i-line product portfolio for Mature markets (≥40nm) • Fab replacement solutions
Circular economy	Sustainable product & service offerings	• System Node Extension Package roadmap • Optimize re-use to secure cost competitive supply

DUV product portfolio to support all market segments

	2020 | 2021 | 2022 | 2023 | 2024 | 2025
ArFi	Continue innovation on advanced NXT platform for improved imaging, overlay and productivity
	Leverage of advanced NXT platform for improved productivity
ArF	Migrate to advanced NXT platform for improved imaging, overlay and productivity
KrF	Productivity increases on XT platform
	Productivity increases on XT platform Migrate to advanced NXT platform for performance and productivity
i-line	Productivity increases on XT platform and migrate to next system for high volume applications

EUV 0.33 NA adoption enabled by platform maturity in high-volume manufacturing



ASML commitment is expected to bring EUV availability >95% and increase wafer per day output >50% by 2025

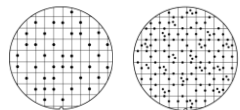
Source : ASML installed base data

EUV

EUV: strategic directions

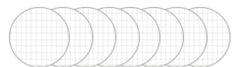
Enabling cost-efficient scaling for advanced nodes

Customer value using EUV



Nanometers

Better device performance: simpler design and superior electrical performance



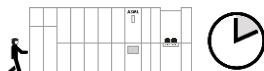
Productivity

Less tools needed to meet fab capacity due to higher throughput

Good wafers per day per cost

Patterning cost saving for critical layers vs alternatives (3x ArFi immersion and above)

Higher yield due to less multiple patterning layers (up to 9%)



Cycle time and time to market

Reduced process complexity leading to shorter learning cycles and faster time-to-yield

ASML EUV product improvements

- Technology roadmap: per node (resolution), improve **imaging, overlay and defectivity (reticle and wafer level)**
- Productivity roadmap over time: increase **Productivity to >200wph, Availability to >97%**

Improvement sub system focus:

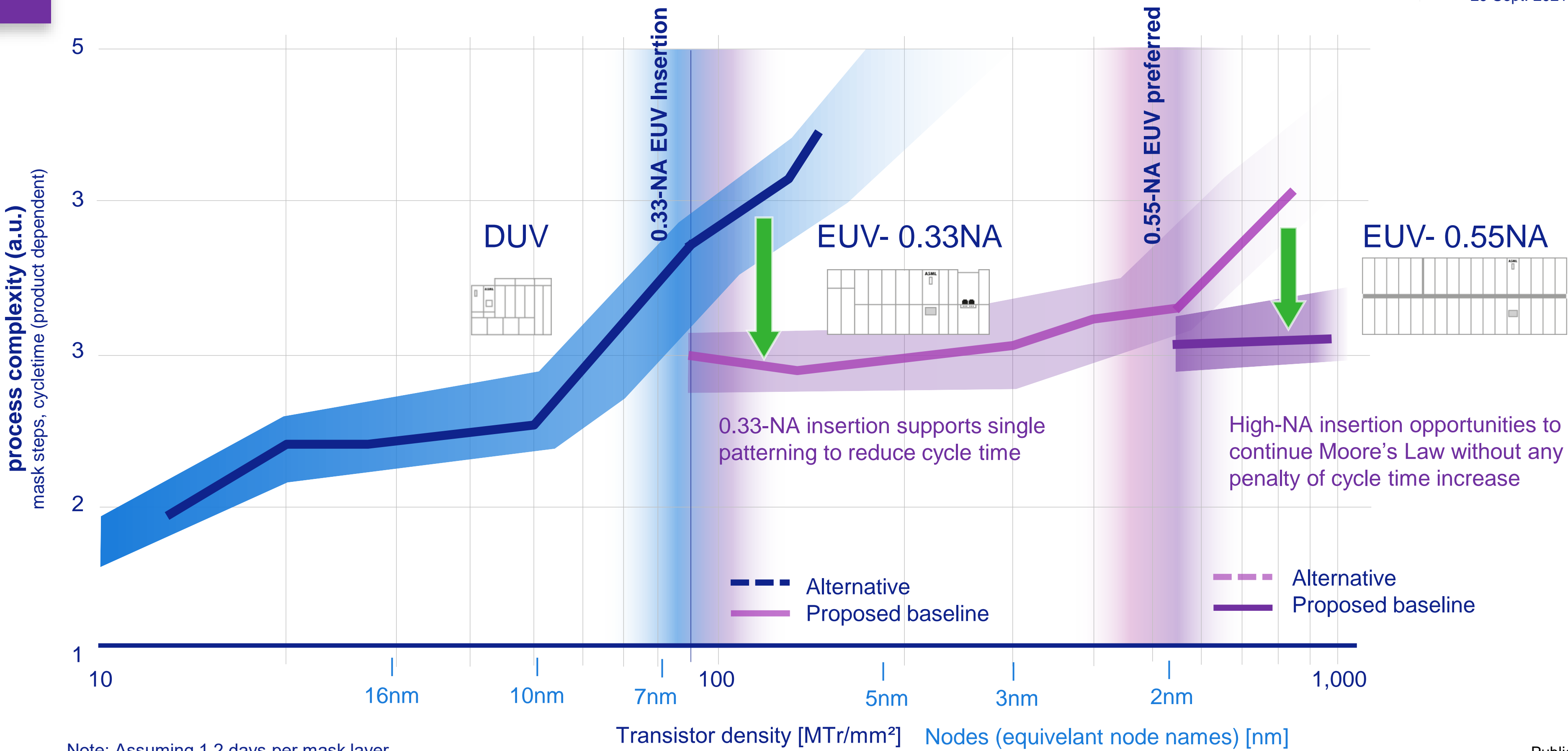
- **Source** (in-line refill, higher power, high reflective mirror)
- **Mirrors** (mirror heating measure, cooled mirrors)
- **Stages and reticle** (Reticle heating, high-accurate fast stages, pellicle durability)
- **Alignment** (# marks, mark size, wafer clamp robustness)

EUV

High-NA to prevent cycle time and process complexity increase

like low NA did for immersion

ASML

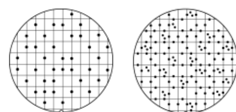


Note: Assuming 1.2 days per mask layer

High-NA EUV: strategic directions

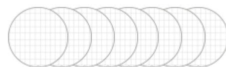
Enabling cost-efficient scaling for next generation advanced nodes

Customer value High-NA EUV



Nanometers

0.55 NA enables 1.7x smaller features and 2.9x increased density



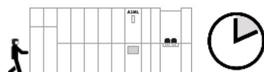
Performance

Higher imaging contrast enables 40% improvement in local CDU
1.4x reduced pattern variability at 1.4x lower dose

Good wafers per day per cost

15% Patterning cost saving for critical layers vs alternatives (2x EUV)

Higher yield due to less multiple patterning layers: 35% less mask count below 2 nm process node



Cycle time and time to market

Reduced process complexity leading to 15% shorter learning cycles and faster time-to-yield

ASML High-NA EUV product improvements

- Technology roadmap: per node (resolution), improve **imaging, overlay and defectivity (reticle and wafer level)**
- Productivity roadmap over time: increase **Productivity**

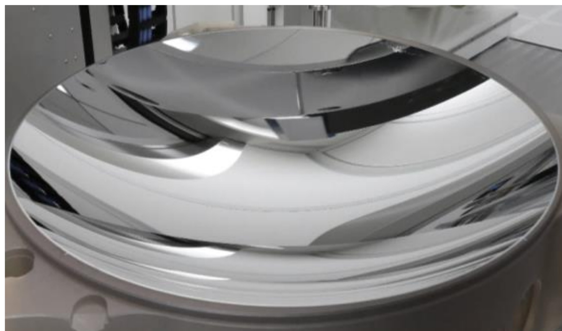
Focus for a successful insertion at our customers

- **Commonality** with existing EUV platform to reduce technological risk, cost of development and switch cost at customer
- **Focus on system maturity and serviceability** to support our customer high volume performance expectation
- Early engagement with our customers to address ecosystems readiness

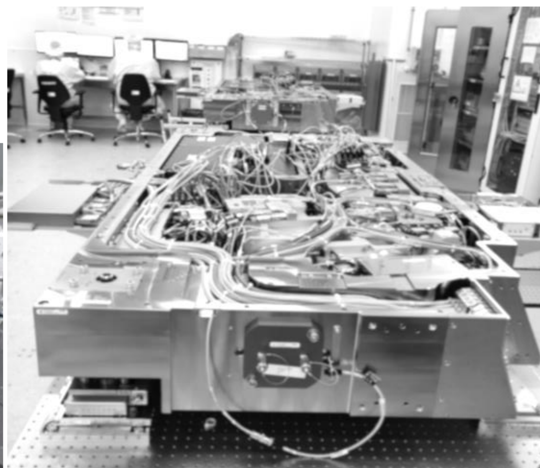
High-NA EUV is in the realization phase

On multiple ASML and supplier locations

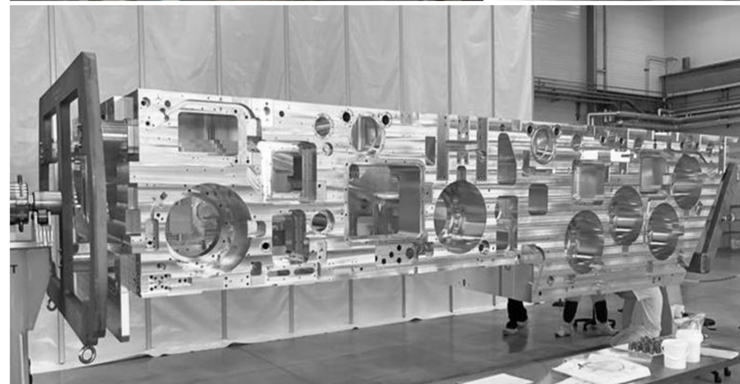
Oberkochen, Germany **optics system manufacturing facilities**



EUV 0.55 NA optics



Veldhoven,
the Netherlands,
system bottom test



Toulon, France, **Frame milling**

Wilton, USA, **system top test**

EUV 0.55 NA is expected to be added to EUV portfolio
for high volume in 2025 - 2026 while continue improving the 0.33 NA platform

	2020	2021	2022	2023	2024	≥2025
EUV	0.33NA continuous imaging, overlay and productivity improvements in line with customers advanced node HVM requirements.					
	0.55NA enabling affordable scaling beyond current decade					

EXE platform, EUV 0.55 NA

NXE platform, EUV 0.33 NA

TRUST

Commonality across EUV, DUV & High-NA platforms

Allows faster and more cost-effective innovation, production and maintenance

Common Technology used in both DUV & EUV platform

DUV

Alignment Sensor
Level sensor
Metrology
Wafer handling

EUV

Common Technology used in DUV products: NXT

NXT (248nm dry)

NXT:870

NXT (193 nm dry)

NXT:1470

NXT (193 nm wet)

NXT:2050i

Common Technology used in both EUV platforms

EUV

Alignment Sensor
Level sensor
Wafer stager
Reticle stager
Wafer handling

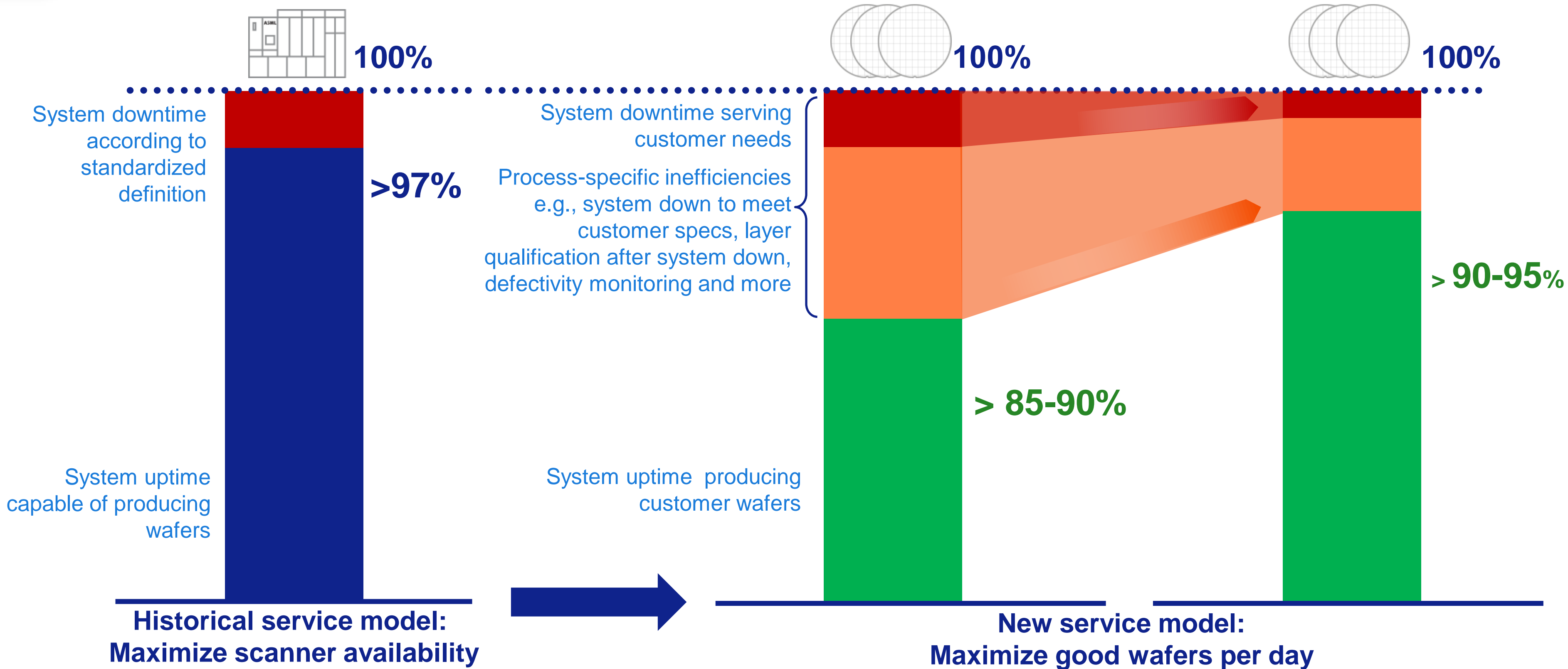
Source
Metrology

EUV High-NA

Maximizing customers' good wafers per day

Next to minimizing system down time

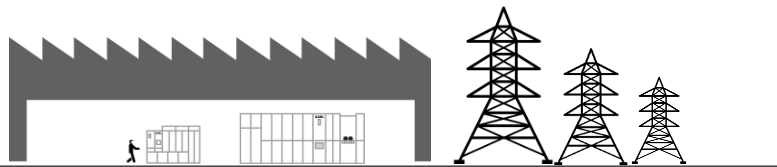
ASML

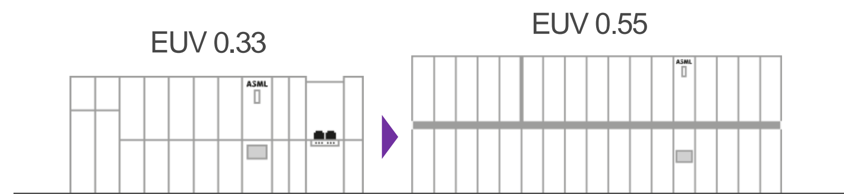


TRUST

EUV is the most energy efficient solution

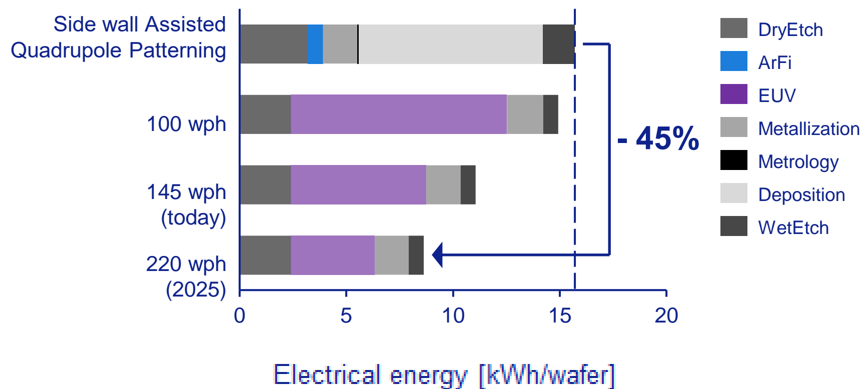
We expect net energy savings of more than 45% over alternative processes





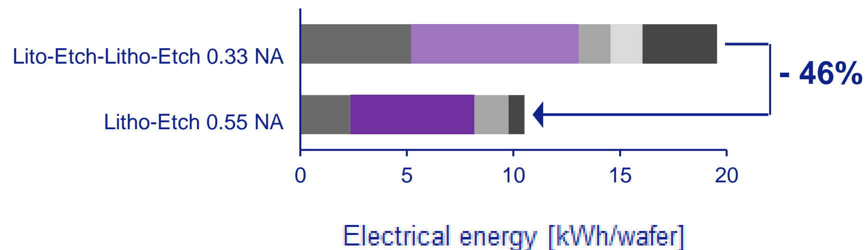
Electrical power reduction

Immersion to EUV 0.33 productivity [wph]



Electrical power reduction

EUV 0.33 to EUV 0.55 at 220 wph



Source: Sri Samavedam a.o., IMEC, “Future of logic scaling: Towards atomic channels and deconstructed chips”, IEDM, Dec 2020, extended by ASML.

Technology strategy
Key messages

- **Moore's Law is alive and well!** Industry innovation continues, fueled by system scaling, delivering highly valued semiconductor products.
- **Semiconductor system scaling** enables exponential performance improvement and energy reduction in support of significant growth of data exchange.
- **Customers' roadmaps** require continued shrink and reduction in edge placement error to drive affordable scaling into next decade.
- **Holistic Lithography roadmap** is driven by our unique patterning control solutions that deliver customer value via improved on product performance.
- **ASML's comprehensive product portfolio** is aligned to our customers' roadmaps, delivering cost effective solutions in support of all applications from leading edge to mature nodes
- **Our next generation EUV technology, High-NA,** is progressing well and will be the engine to drive the lithography roadmap into the next decade
- **Continued execution of our strategic priorities** is expected to provide cost effective solutions for our customers, enable the extension of the industry roadmap into the next decade, and support our long-term sustainability commitment

Forward Looking Statements

This presentation contains statements that are forward-looking, including statements with respect to expected industry and business environment trends including expected growth, outlook and expected financial results, including expected net sales, gross margin, R&D costs, SG&A costs and effective tax rate, annual revenue opportunity for 2025, financial model for 2025 and assumptions and expected growth rates and drivers, expected growth including growth rates 2020-2025 and 2020-2030, total addressable market, growth opportunities beyond 2025 and expected annual growth rate in lithography and metrology and inspection systems and expected annual growth rate in installed base management, expected trends in addressable market up to 2030, expected trends in Logic and Memory revenue opportunities, long term growth opportunities and outlook, expected trends in demand and demand drivers, expected benefits and performance of systems and applications, semiconductor end market trends, expected growth in the semiconductor industry including expected demand growth and capital spend in coming years, expected wafer demand growth and investments in wafer capacity, expected lithography market demand and growth and spend, growth opportunities and drivers, expected trends in EUV and DUV demand, sales, outlook, roadmaps, opportunities and capacity growth and expected EUV adoption, profitability, availability, productivity and output and estimated wafer demand and improvement in value, expected trends in the applications business, expected trends in installed base management including expected revenues and target margins, expected trends and growth opportunity in the applications business, expectations with respect to high-NA, the expectation of increased output capacity, plans, strategies and strategic priorities and direction, expectation to increase capacity, output and production to meet demand, the expectation that Moore's law will continue and Moore's law evolution, product, technology and customer roadmaps, and statements and intentions with respect to capital allocation policy, dividends and share buybacks, including the intention to continue to return significant amounts of cash to shareholders through a combination of share buybacks and growing annualized dividends and statements with respect to ESG commitment, sustainability strategy, targets, initiatives and milestones. You can generally identify these statements by the use of words like "may", "will", "could", "should", "project", "believe", "anticipate", "expect", "plan", "estimate", "forecast", "potential", "intend", "continue", "target", "future", "progress", "goal" and variations of these words or comparable words. These statements are not historical facts, but rather are based on current expectations, estimates, assumptions and projections about our business and our future financial results and readers should not place undue reliance on them. Forward-looking statements do not guarantee future performance and involve a number of substantial known and unknown risks and uncertainties. These risks and uncertainties include, without limitation, economic conditions; product demand and semiconductor equipment industry capacity, worldwide demand and manufacturing capacity utilization for semiconductors, semiconductor end-market trends, the impact of general economic conditions on consumer confidence and demand for our customers' products, performance of our systems, the impact of the COVID-19 outbreak and measures taken to contain it on the global economy and financial markets, as well as on ASML and its customers and suppliers, and other factors that may impact ASML's sales and gross margin, including customer demand and ASML's ability to obtain supplies for its products, the success of R&D programs and technology advances and the pace of new product development and customer acceptance of and demand for new products, production capacity and our ability to increase capacity to meet demand, the number and timing of systems ordered, shipped and recognized in revenue, and the risk of order cancellation or push out, production capacity for our systems including the risk of delays in system production and supply chain capacity, constraints, shortages and disruptions, trends in the semi-conductor industry, our ability to enforce patents and protect intellectual property rights and the outcome of intellectual property disputes and litigation, availability of raw materials, critical manufacturing equipment and qualified employees and trends in labor markets, geopolitical factors, trade environment; import/export and national security regulations and orders and their impact on us, ability to meet sustainability targets, changes in exchange and tax rates, available liquidity and liquidity requirements, our ability to refinance our indebtedness, available cash and distributable reserves for, and other factors impacting, dividend payments and share repurchases, results of the share repurchase programs and other risks indicated in the risk factors included in ASML's Annual Report on Form 20-F for the year ended December 31, 2020 and other filings with and submissions to the US Securities and Exchange Commission. These forward-looking statements are made only as of the date of this document. We undertake no obligation to update any forward-looking statements after the date of this report or to conform such statements to actual results or revised expectations, except as required by law.

ASML
Small
Talk
2021
Investor Day
Virtual
ASML