ASML

Small Talk 2024

Global market trends
Industry & ASML's technology roadmap
ESG

Christophe Fouquet
President and Chief Executive Officer

ASML Investor Day
Veldhoven, The Netherlands
November 14, 2024

We expect that our ability to scale EUV technology into the next decade and extend our versatile holistic lithography portfolio could place ASML at the heart of the AI opportunity. This would continue to create significant growth in revenue and profitability in this decade.

- The Semiconductor Industry remains strong and Artificial Intelligence is expected to create further opportunity as major investments in supercomputing are happening and the entire industry is preparing to insert AI in all critical future applications
- Our industry will require major innovations to address the anticipated cost and power consumption challenges of AI, and this will further boost the industry roadmap in a product mix shifting towards advanced logic and DRAM
- Our customers remain at the core of our strategy, and we believe that lithography will remain at the heart of their innovation. We also anticipate that an increased number of critical lithography exposures for advanced logic and memory processes will continue to support our customers in addressing their challenges
- We expect that our ability to 1- scale our EUV technology well into the next decade, 2- extend holistic lithography into supporting 3D front end integration and 3- improve the performance and cost effectiveness of our DUV products will continue to address all our customers' needs with a flexible and versatile portfolio
- We will continue to leverage our large and growing systems installed base (DUV, EUV) to provide high value service and upgrades over a >20 years lifetime
- ASML values the strong industry partnerships which are critical to our success and our collective commitment to a leadership position in ESG

Customer trust and partnership remains at the core of ASML's strategy

We expect that our ability to scale EUV technology into the next decade and extend our versatile holistic lithography portfolio could place ASML at the heart of the AI opportunity. This would continue to create significant growth in revenue and profitability in this decade.

SK hynix **Seon-Yong Cha, SK Hynix CTO**

We see our society going from chips everywhere to AI chips everywhere

Gen AI opens endless opportunities, expected to add 6-13T$ value to GDP by 2030

Connected world

- Hyperconnectivity
- Cloud infrastructure
- Internet of Things
- Edge computing

Climate change and resource scarcity

- Energy transition
- Electrification, smart mobility
- Agricultural innovation
- Smarter use of limited resources

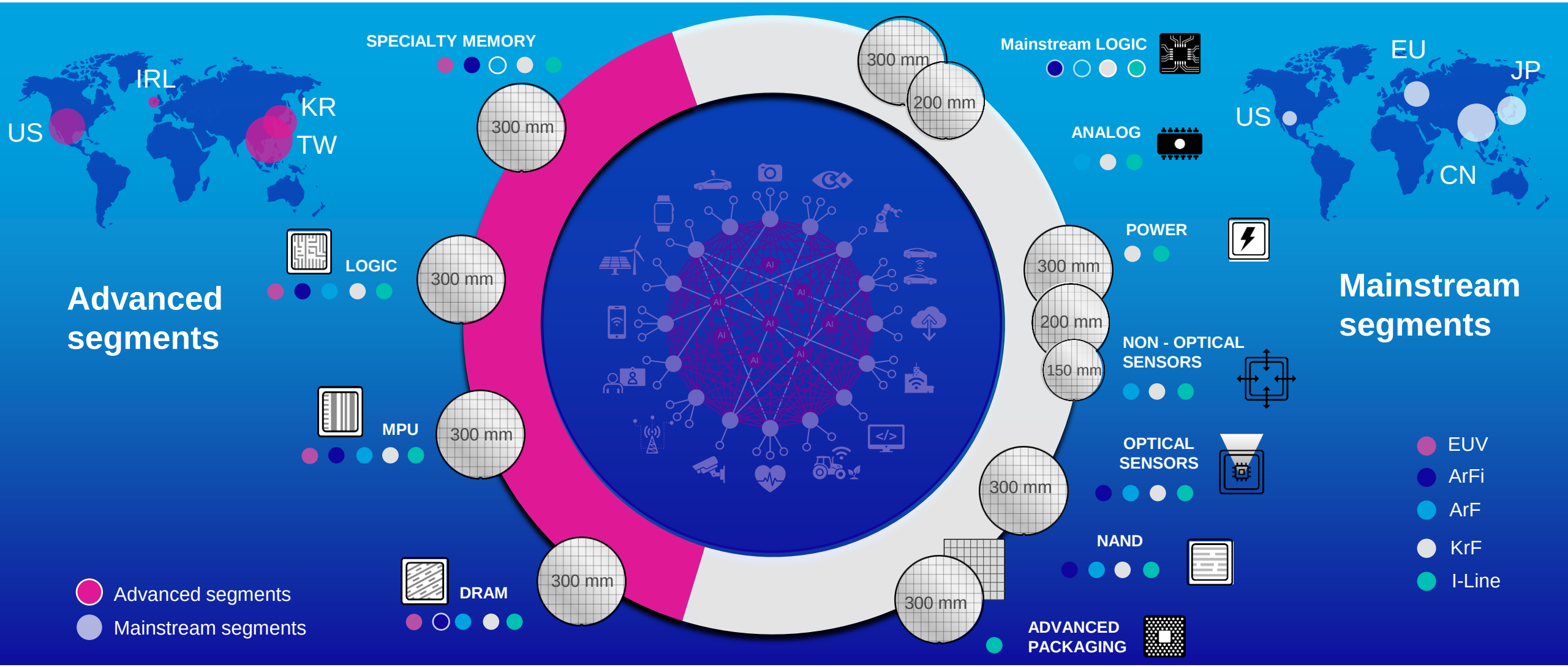
Social and economic shifts

- Working, learning remotely
- Healthcare, medical tech
- Technological sovereignty
- Automation

*Source: McKinsey and Company, GenAI: The next S-curve for the semiconductor industry? | March 2024

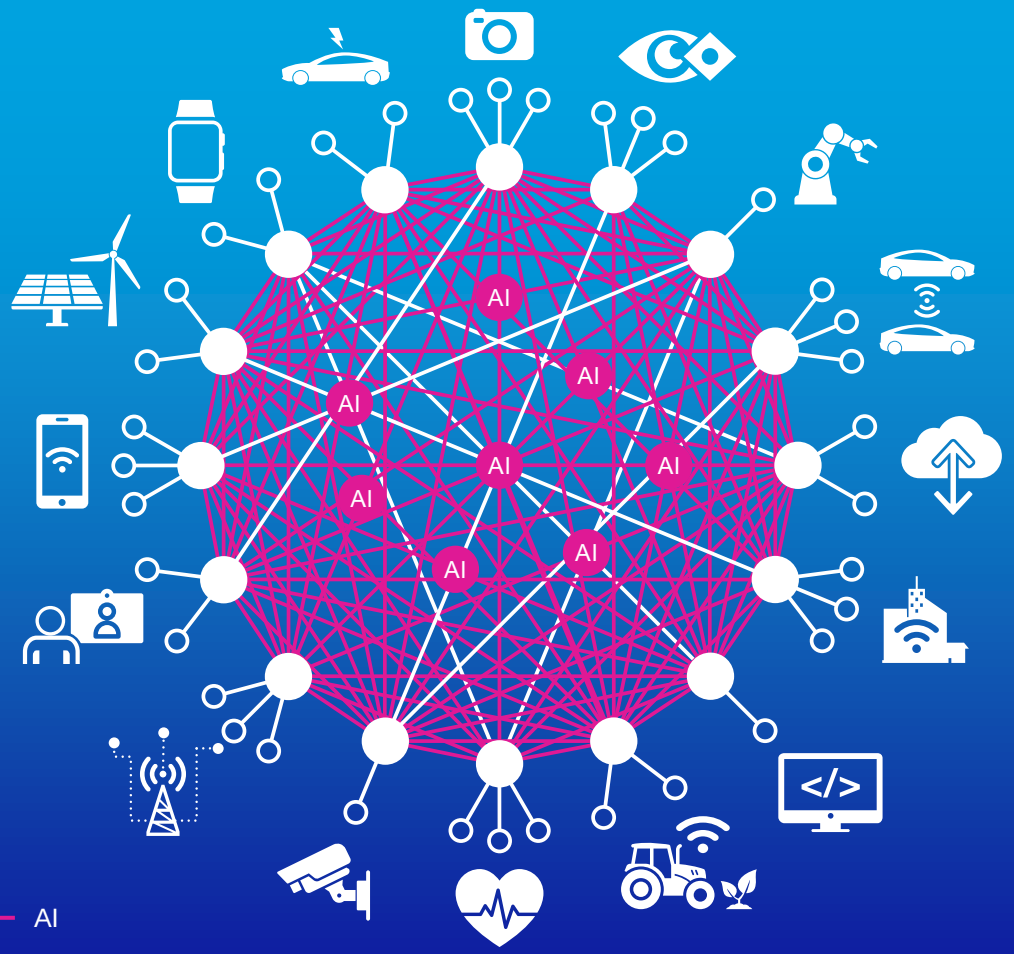
AI has strong potential to drive entire industry forward across many applications

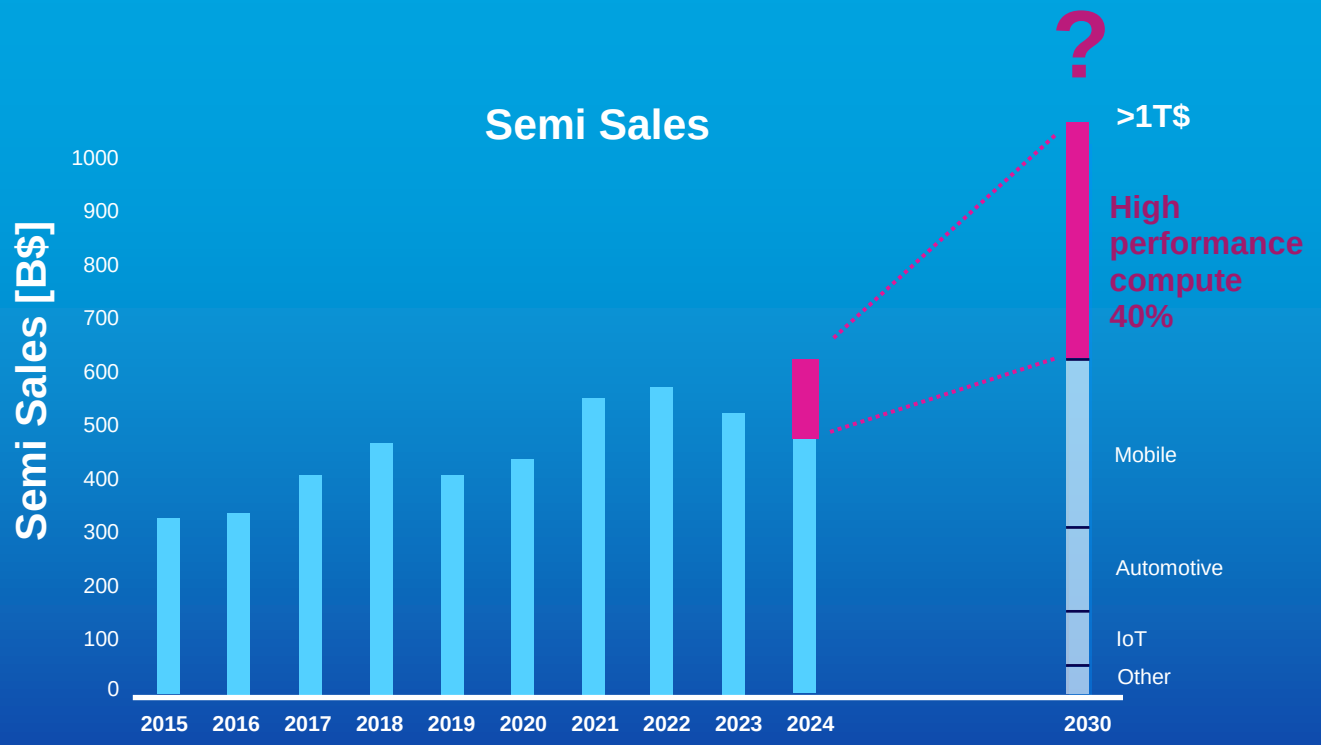
Mainstream markets grow in volume while high performance continues to follow Moore's law



We reconfirm our view calling for global semi sales >$1T by 2030

Major investments are on-going in AI, the exact pace of its roll-out to consumer products is still unknown





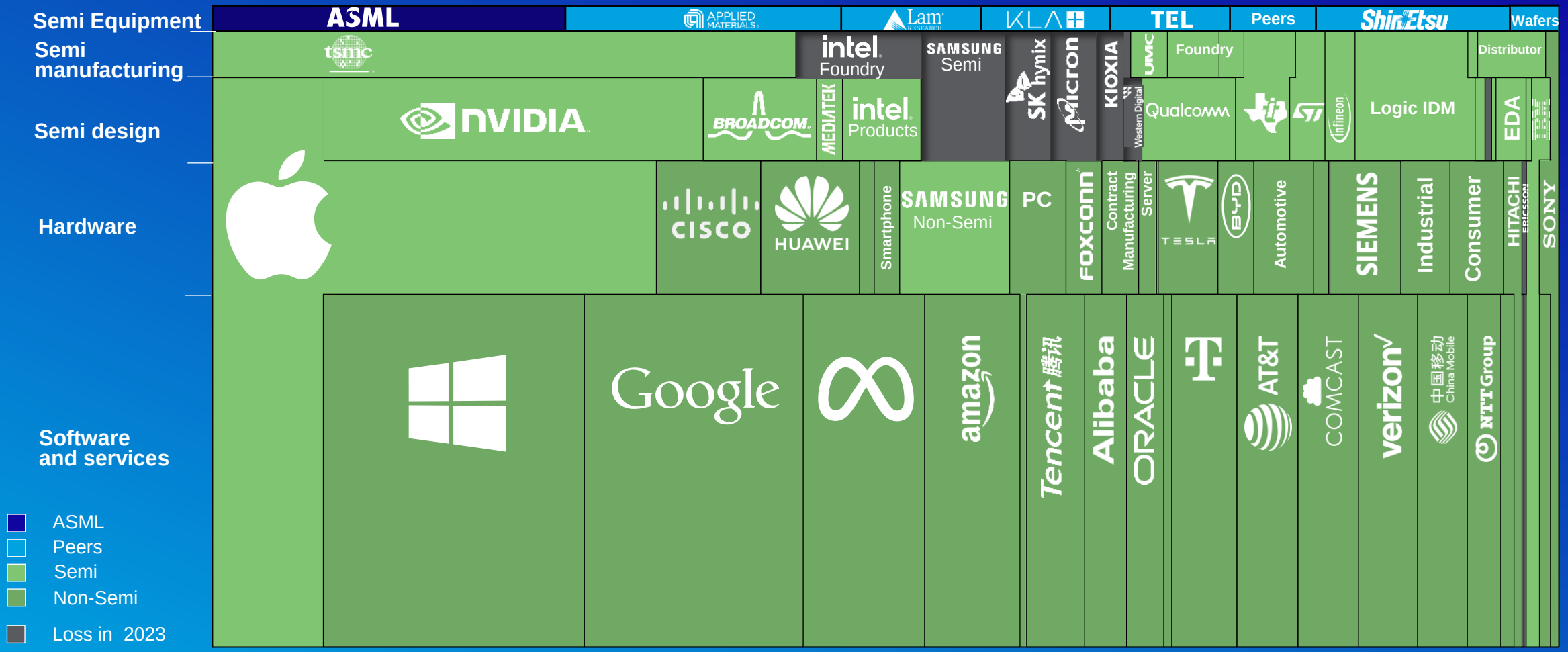
Global data center and edge AI demands are expected to grow significantly year on year to represent >40% of semi sales demand in 2030 and generate some upside for our industry

AI
Connecting IoT
Sensors
Mainstream edge compute
Data AI power compute (+memory)

*Source: Kevin Zhang, TSMC, Semiconductor Industry: Present and Future, IEEE solid state Circuit Conference, Feb 2024
*Source: McKinsey and Company, GenAI: The next S-curve for the semiconductor industry? | March 2024
*Source: WSTS and Gartner

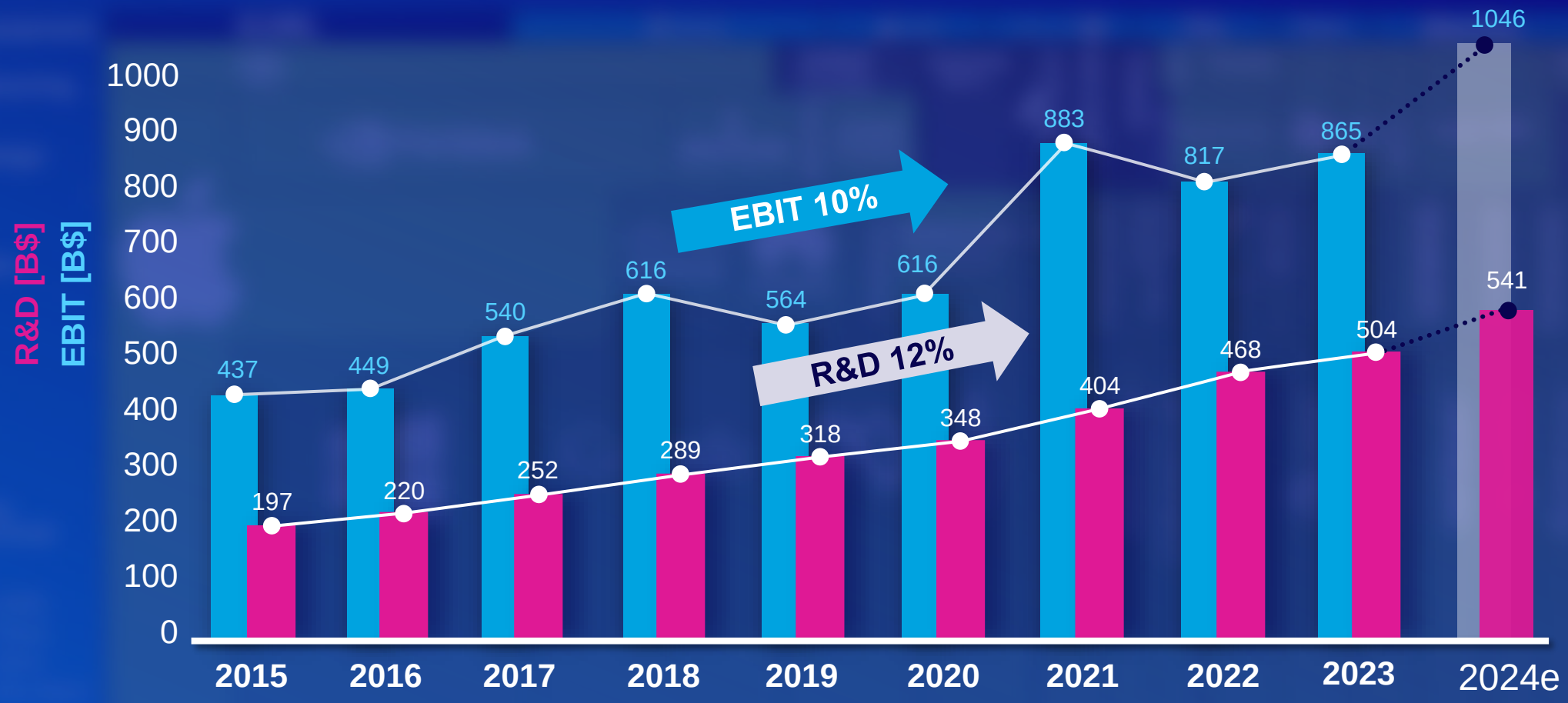
The semiconductor ecosystem has considerable means to drive innovation

Despite a market downturn, the ecosystem generated over $865B EBIT in 2023



Source: Corporate Marketing (CMKT) analysis; Company reports; Note: EBIT = Earnings before Interest & Taxes. Box size scales to EBIT

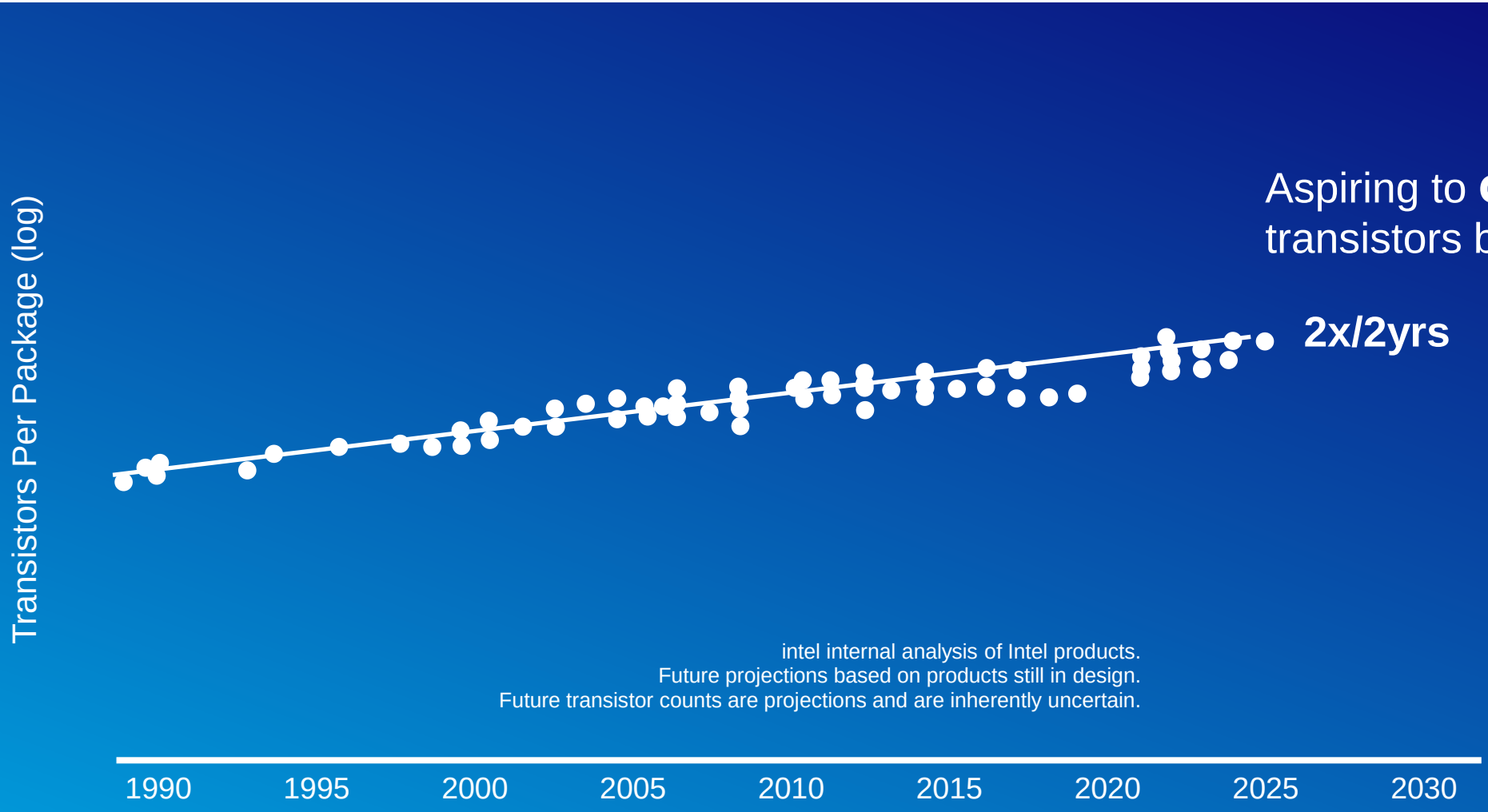
The semiconductor ecosystem has reinvested around half of its EBIT to drive long-term innovation and growth, and we expect this to continue



Source: Corporate Marketing (CMKT) analysis; Company reports; Note: EBIT = Earnings before Interest & Taxes.

Moore’s law for computing power is alive and well

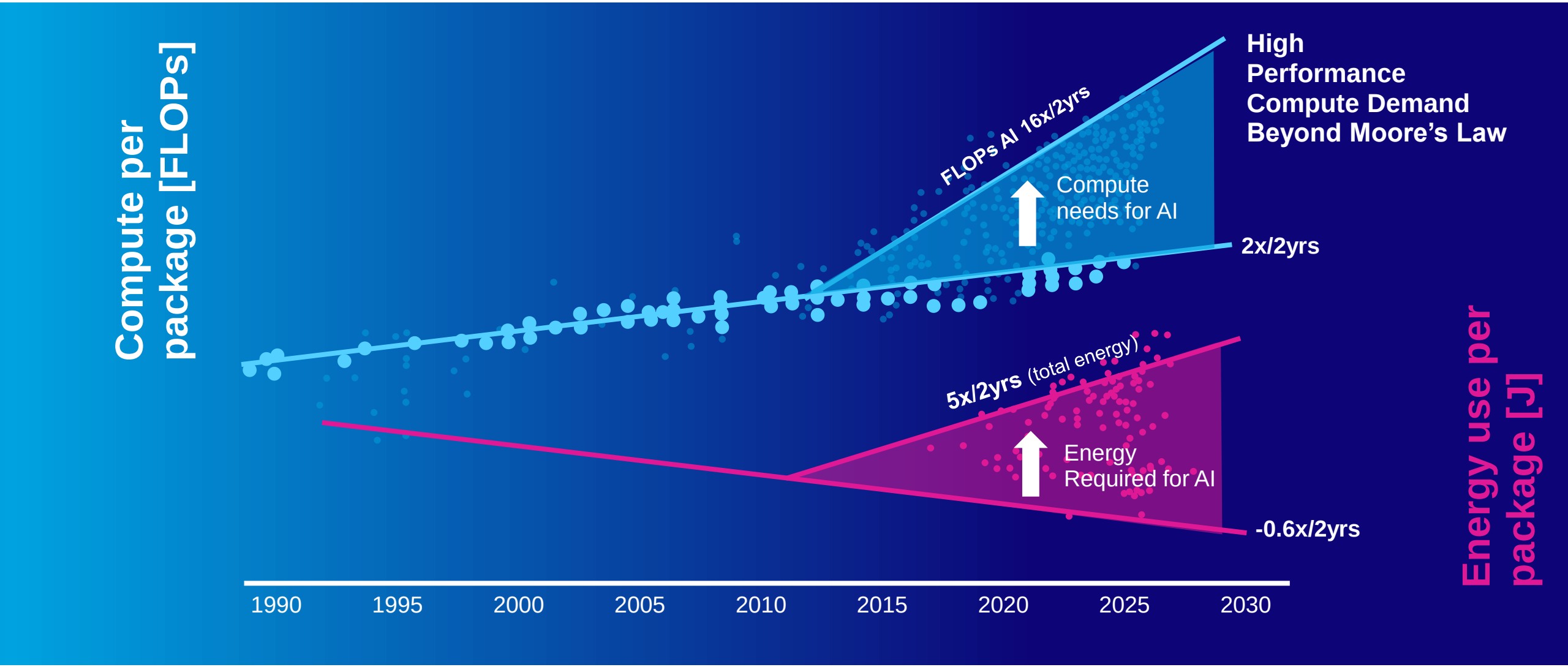
Transistors per package continue to double every two years enabling one trillion by 2030



Source: Ann Kelleher, Intel, “Moore’s law – now and in the future”, Intel investor day Feb 17, 2022

We expect that Generative AI will demand an acceleration of Moore's law

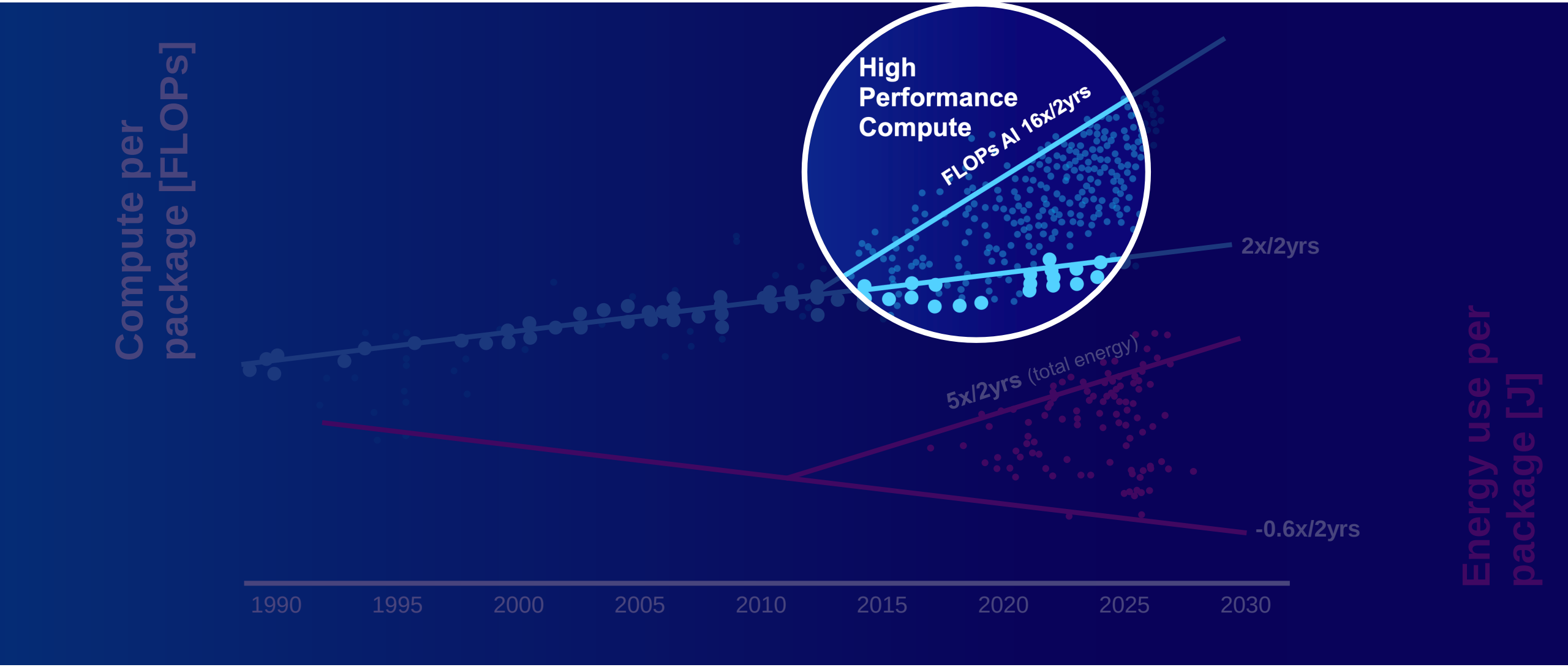
Energy use could set a ceiling on training capability moving forward if not addressed



Source: High Performance Computing: https://top500.org/lists/top500/ based on FP64 performance; Consumer GPU: nVidia & AMD data sheets based on FP32 performance
Source: EPOCH AI, " Notable AI models" June 2024, updated Nov 2024

Generative AI, high-performance computing power outpaces Moore's law

In 2030, >70% of data center demand could be driven by AI, representing >90% of Gen AI FLOPs

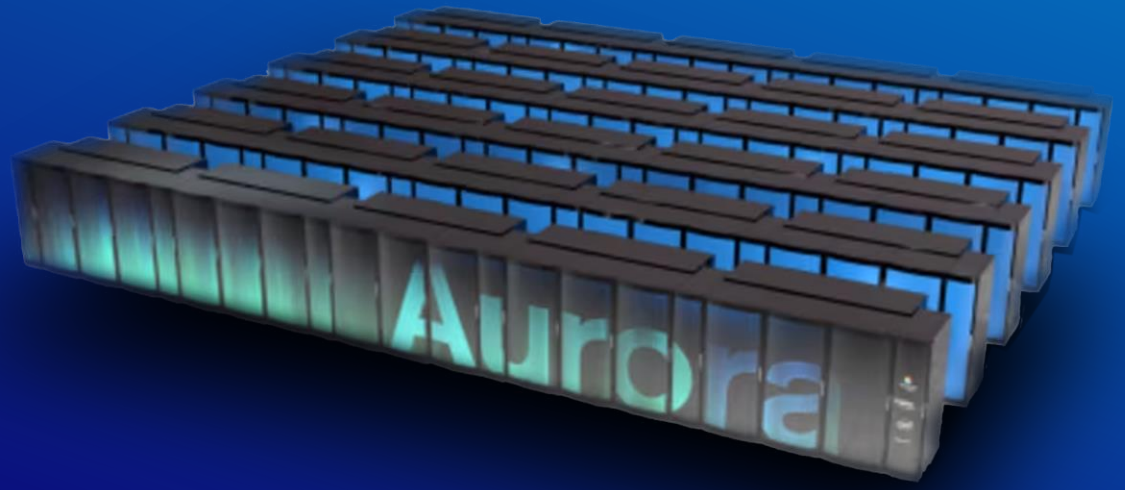


Source: High Performance Computing: https://top500.org/lists/top500/ based on FP64 performance; Consumer GPU: nVidia & AMD data sheets based on FP32 performance
Source: EPOCH AI, " Notable AI models" June 2024, updated Nov 2024

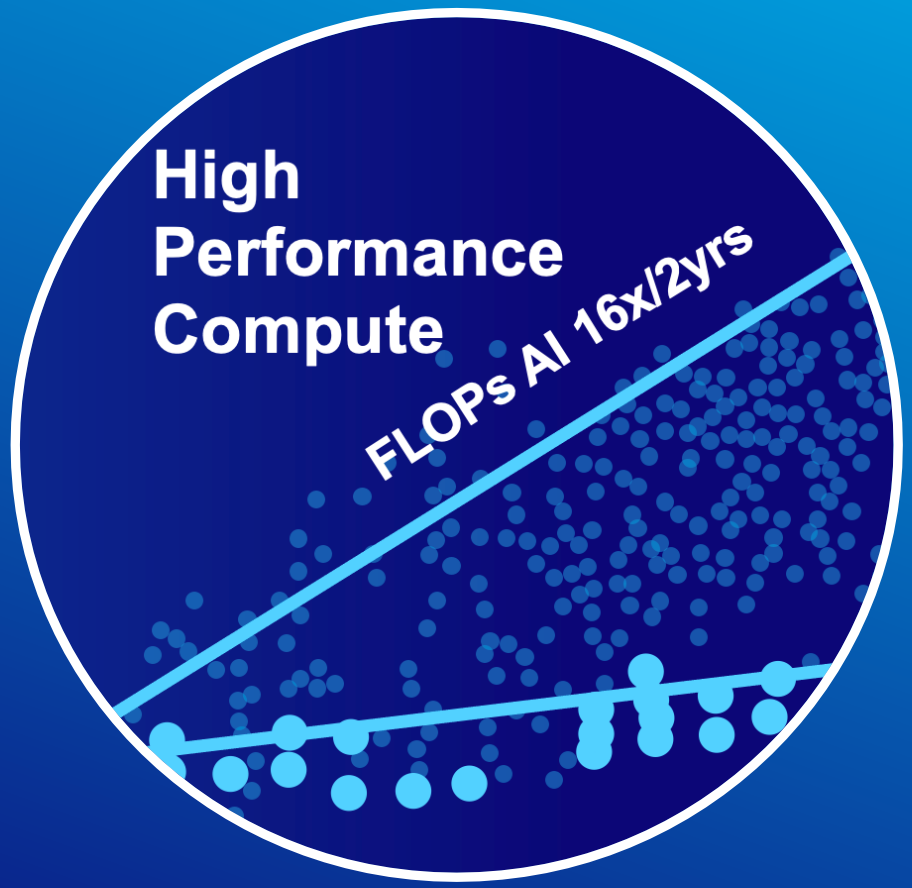
Generative AI, high-performance computing power outpaces Moore's law

Supercomputer architecture has the potential to meet the needs of AI

High-performance computing



Aurora supercomputer (HPC and AI applications) **delivers 2,000,000,000,000,000,000 FLOPs**

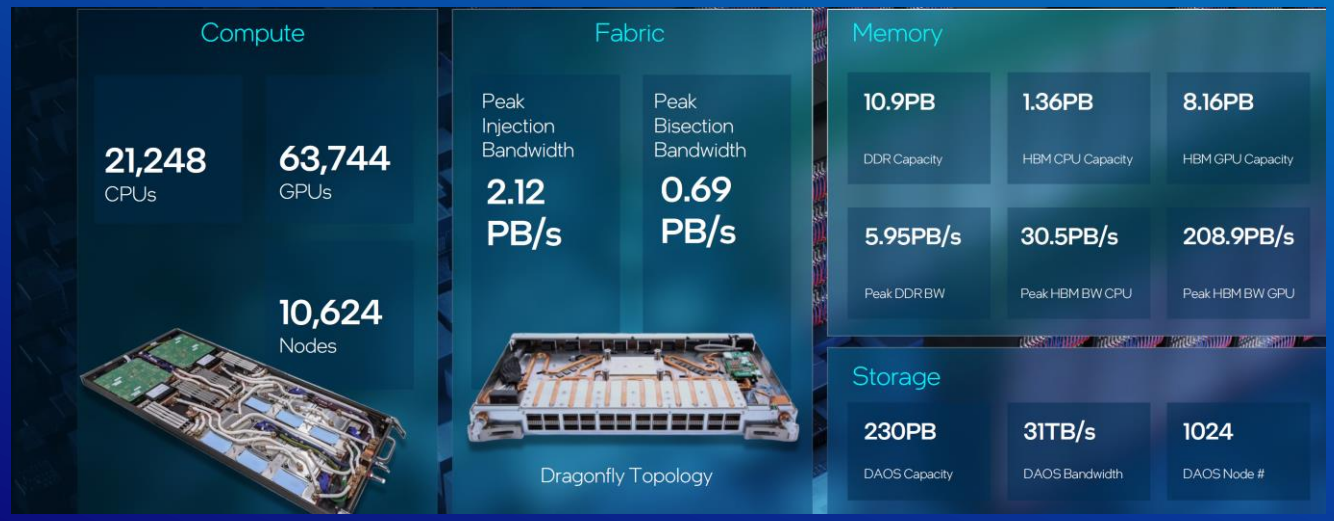


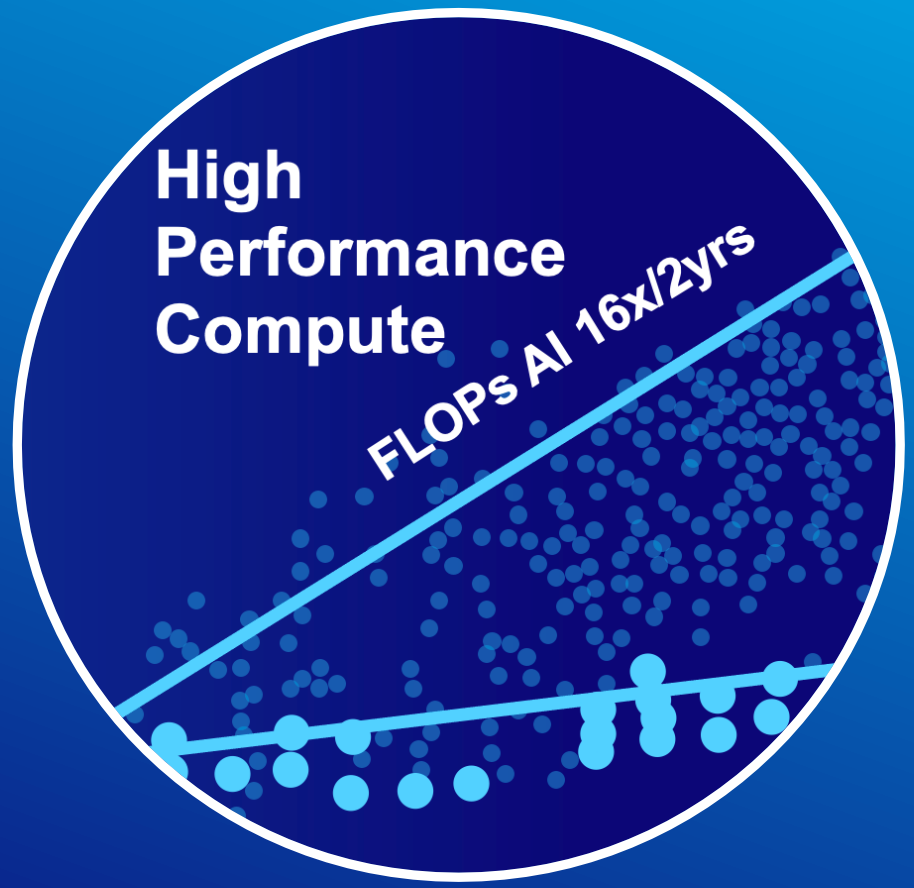
Argonne Leadership Computing Facility: https://www.alcf.anl.gov/aurora

Generative AI, high-performance computing power outpaces Moore's law

Architecture cost must be reduced to fully enable AI opportunity

Cost: >500M$





Aurora supercomputer (HPC and AI applications)
delivers 2,000,000,000,000,000,000 FLOPs

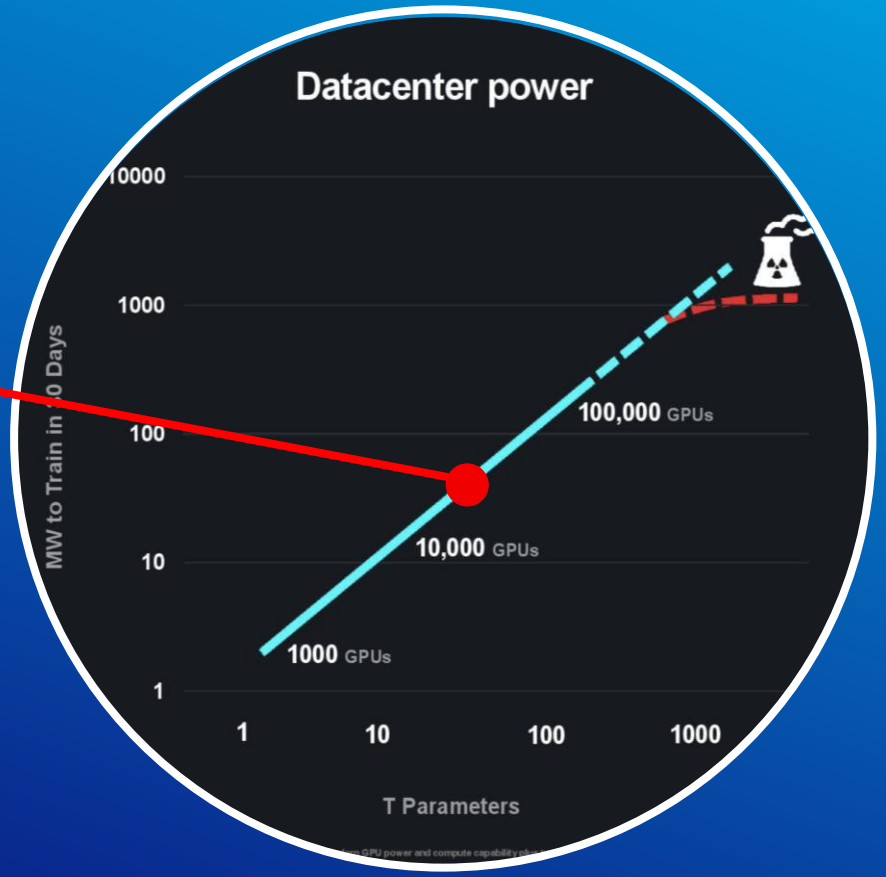
using ~85K CPUs/GPUS, >20PB memory for computing and >230PB memory for storage at ~500 M$ cost

Argonne Leadership Computing Facility: https://www.alcf.anl.gov/aurora

Generative AI, high-performance computing power outpaces Moore's law

HPC rapidly growing energy consumption must be addressed to prevent a ceiling on training capability

Energy consumption: >60MW



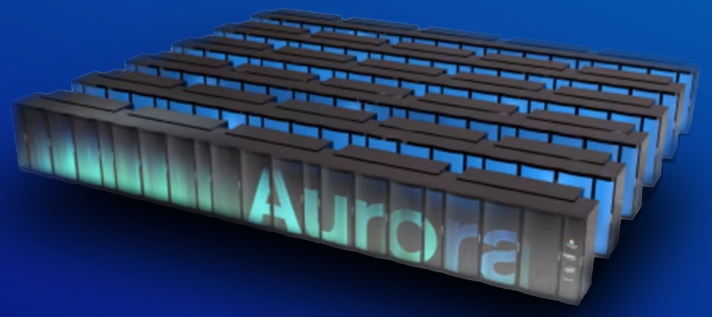
Aurora supercomputer (HPC and AI applications)
delivers **2,000,000,000,000,000,000 FLOPs**

using 60MW and 34,000 gallons of water per minute for cooling

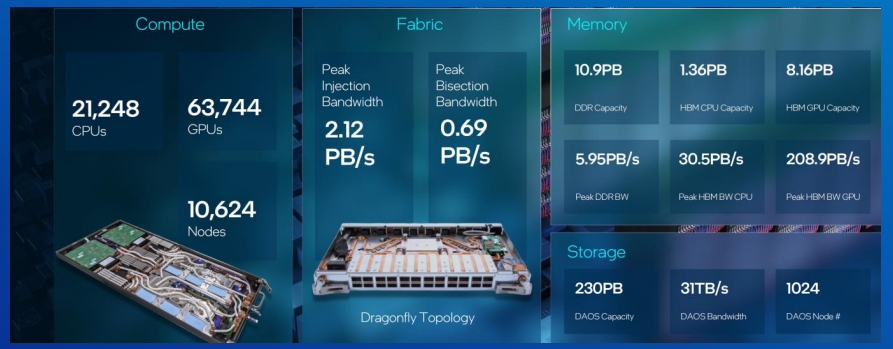
Argonne Leadership Computing Facility: https://www.alcf.anl.gov/aurora. | Source : Lisa Su, AMD, ITF May 21 2024

Scalability of High-performance computing is endless..
… but new cost and energy challenges must be met to unleash AI opportunity

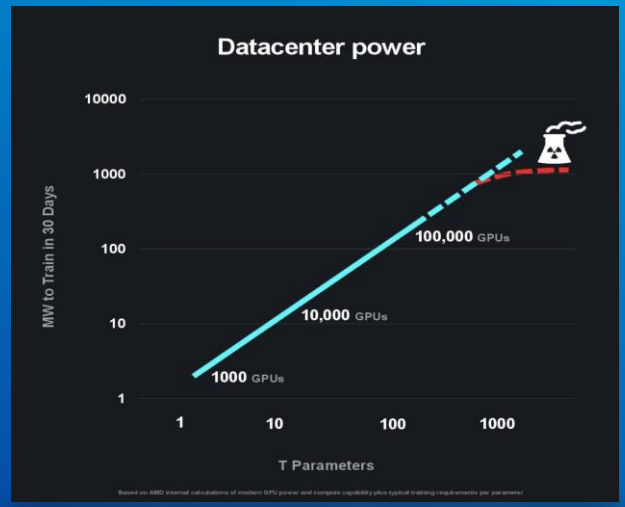
AI computing architecture[1]



AI architecture cost[2]



AI energy consumption[3]



2 exa FLOPS

Cost estimate: ~500M$

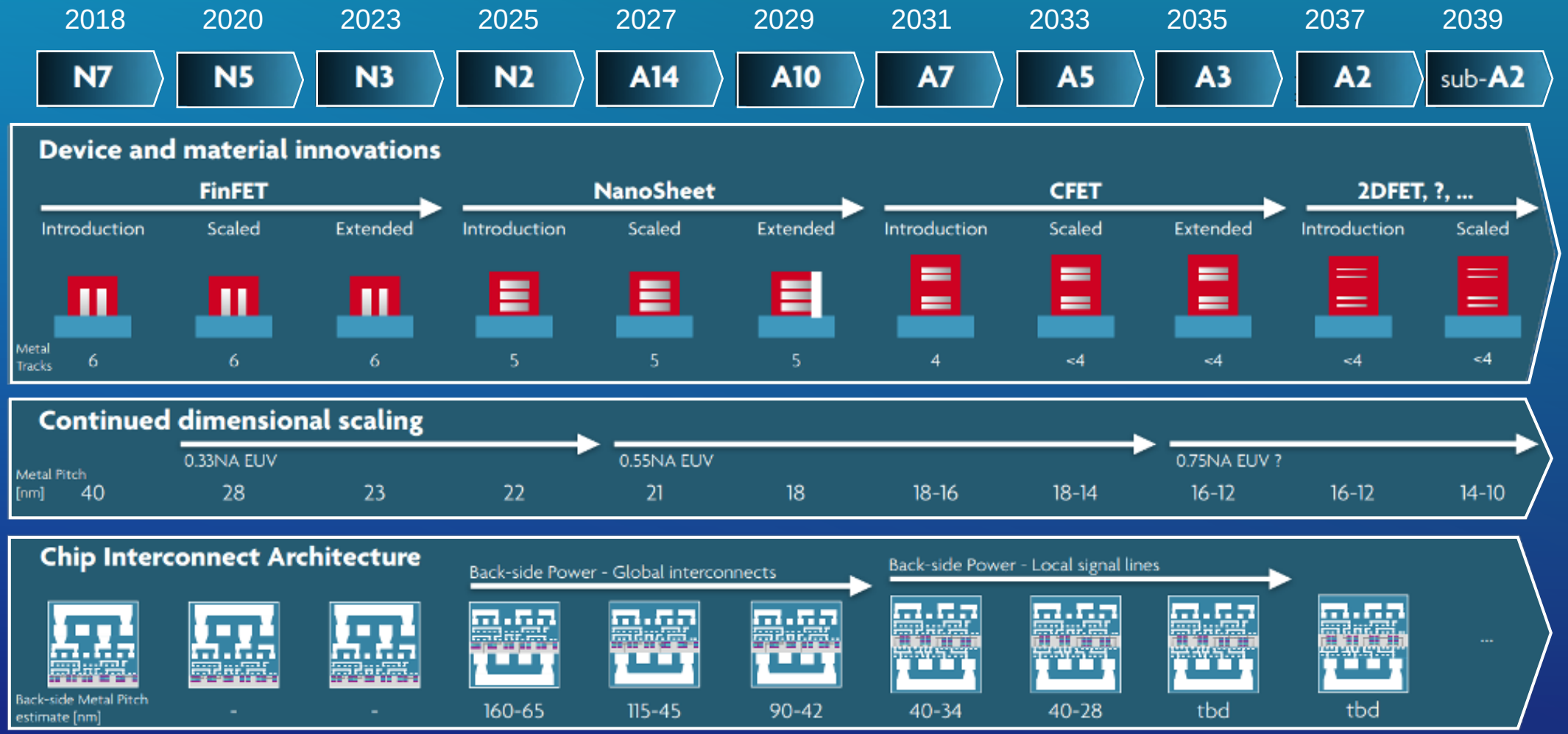
60MW

The semiconductor industry needs to deliver the highest computing power / transistor density at the lowest cost, including the lowest possible CO_2 emission

Source:Lisa Su, AMD, ITF May 21 2024
Argonne Leadership Computing Facility: https://www.alcf.anl.gov/aurora

We expect AI applications to accelerate the need for advanced logic roadmap

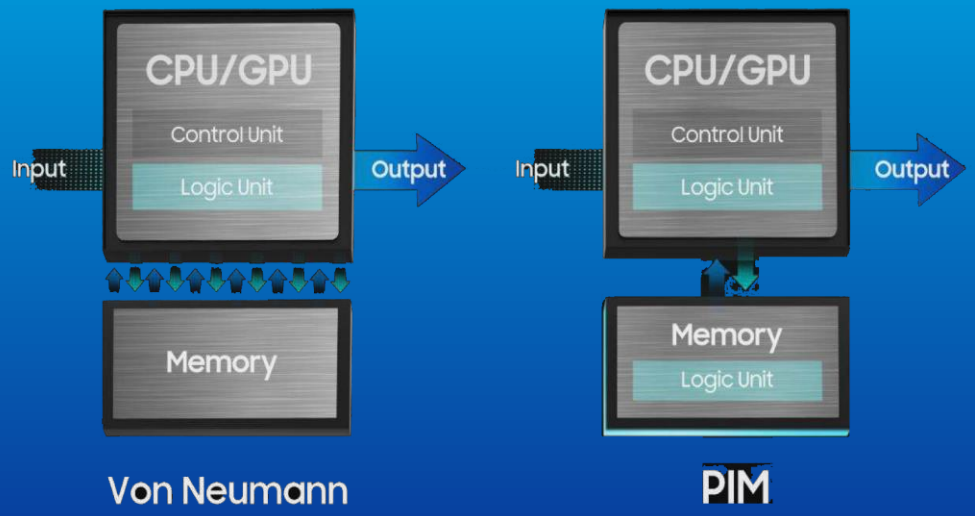
Future 2D and 3D innovations are paving the way for the next 15 years



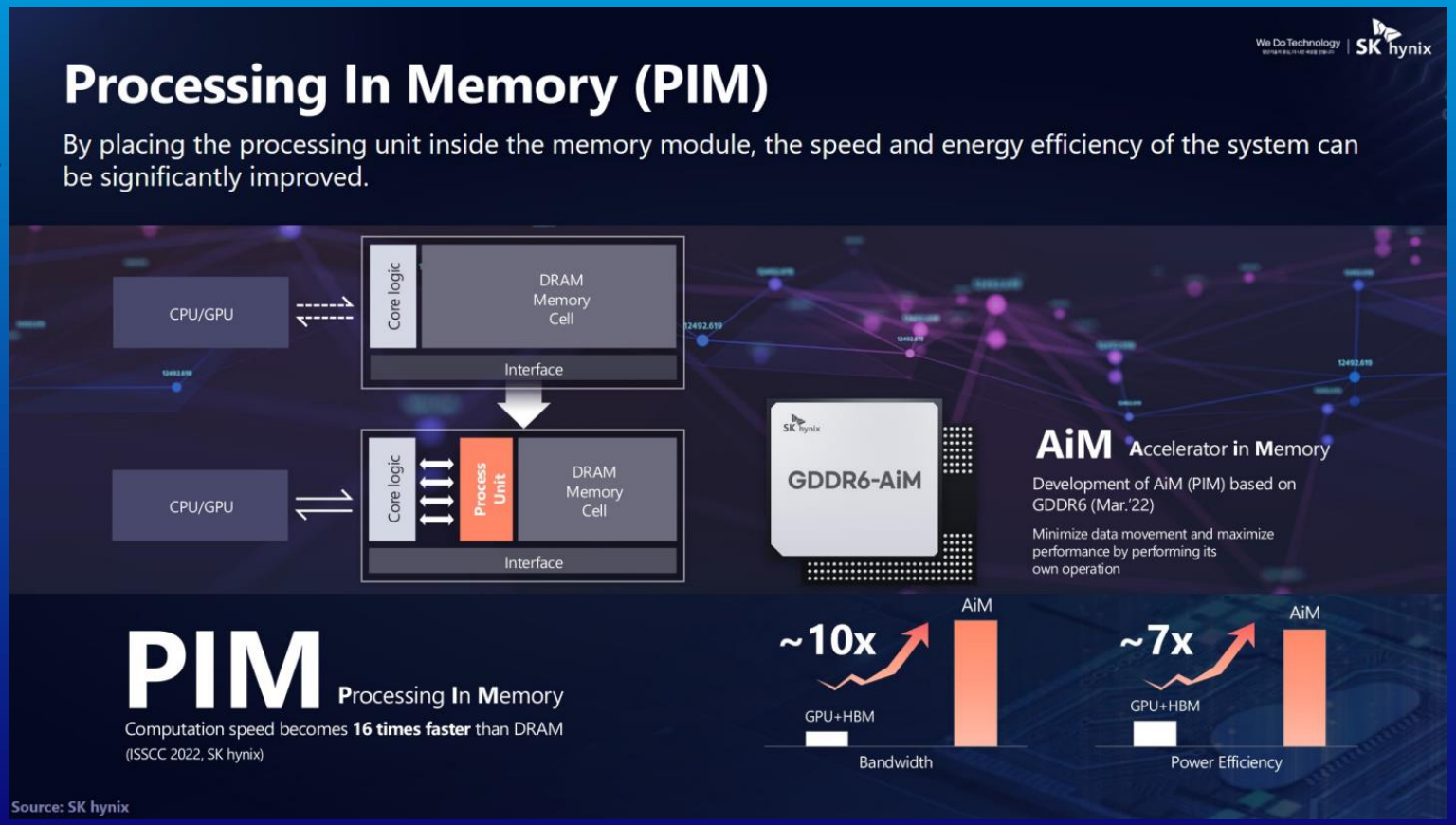
imec

We expect AI applications to transform DRAM architecture and volume

Future DRAM should integrate additional logic functionalities to improve performance & energy efficiency

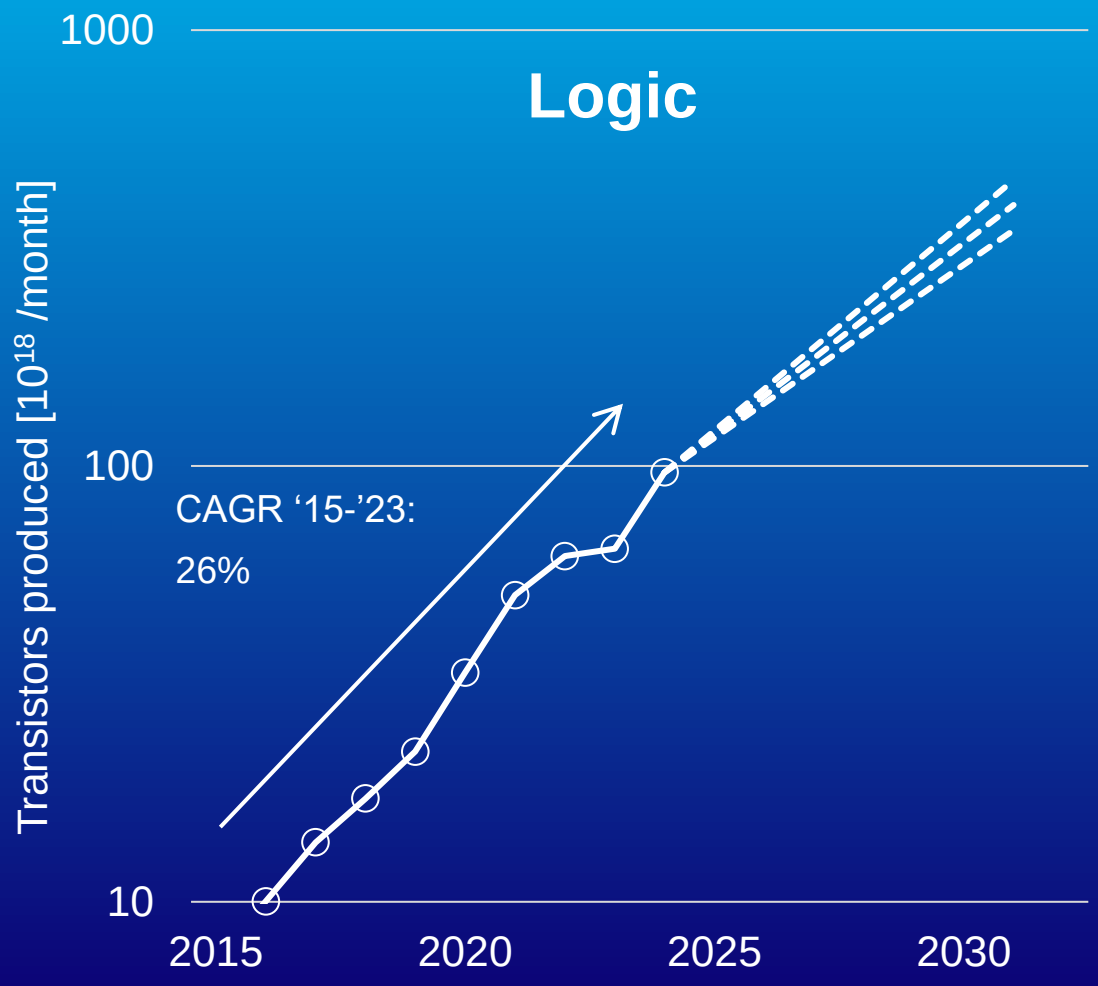


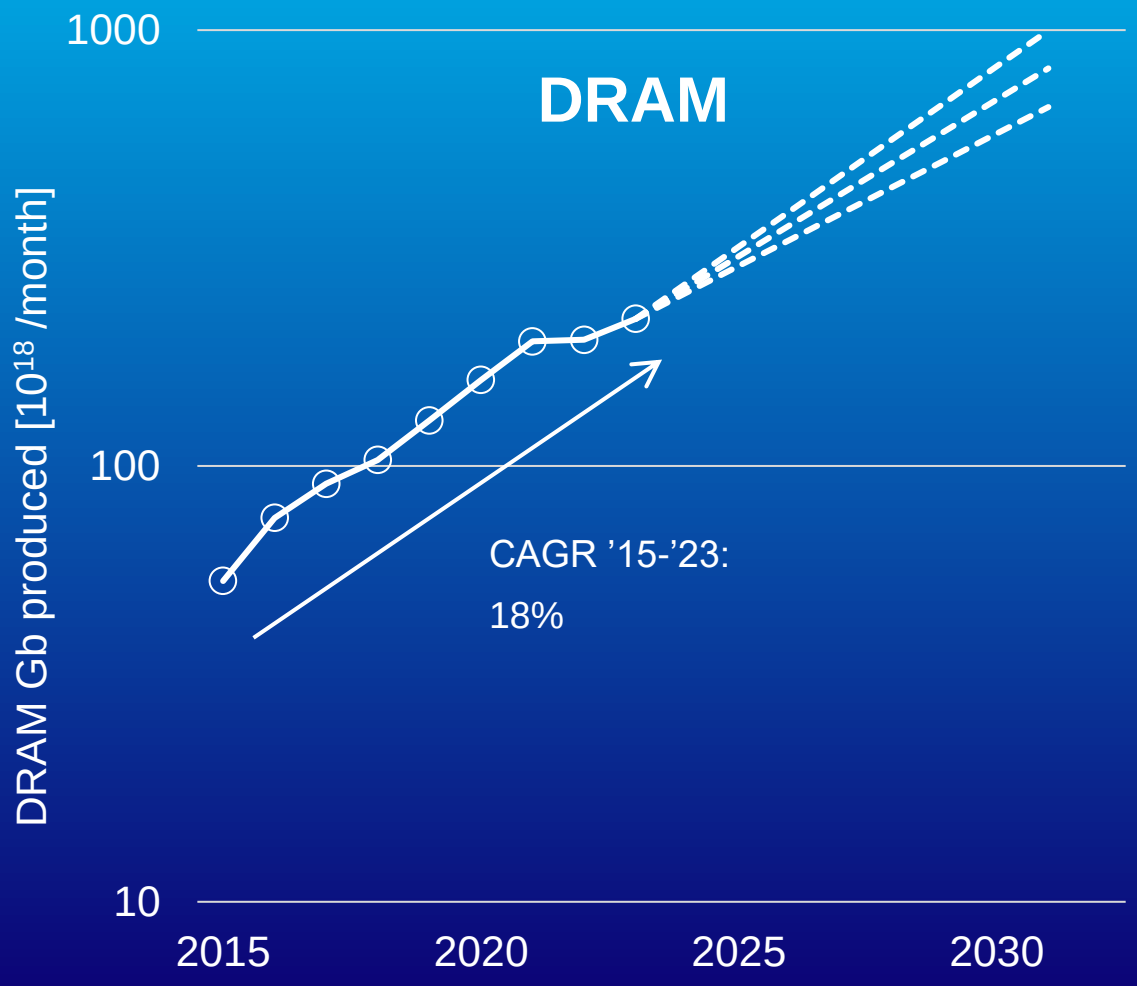
"PIM can improve performance and energy efficiency of memory-bound workloads by adding additional logic functionality to DRAM memory"



So, we continue to anticipate strong transistor growth for both logic and DRAM

And we expect the semiconductor demand mix to shift towards advanced logic and DRAM

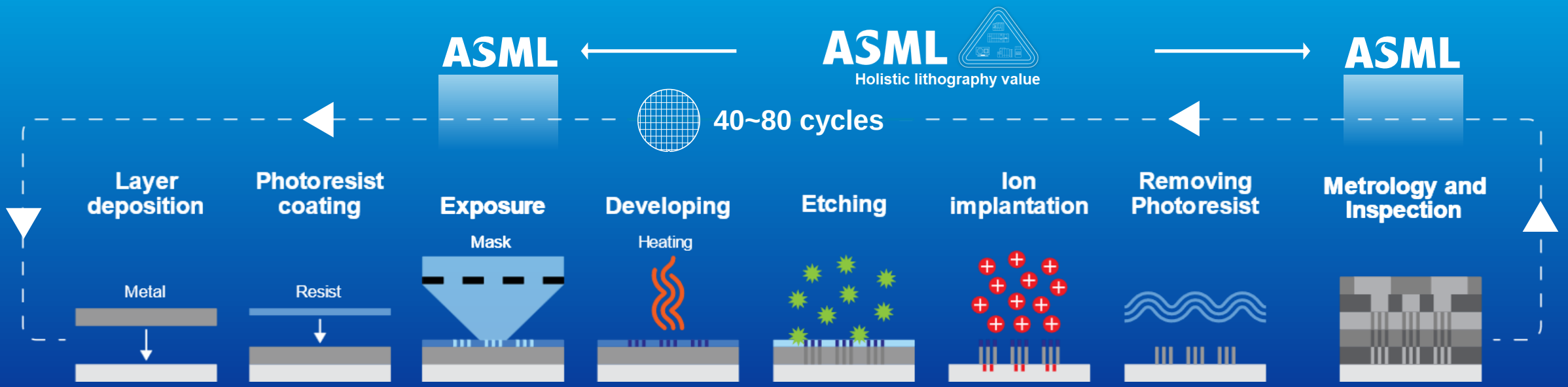




Source: Logic history: ASML end market model, DRAM history: WSTS, projections: ASML

Cost and energy reduction should be at the core of future process optimization

Total cost and total emissions of wafer patterning must be reduced to support AI roadmap

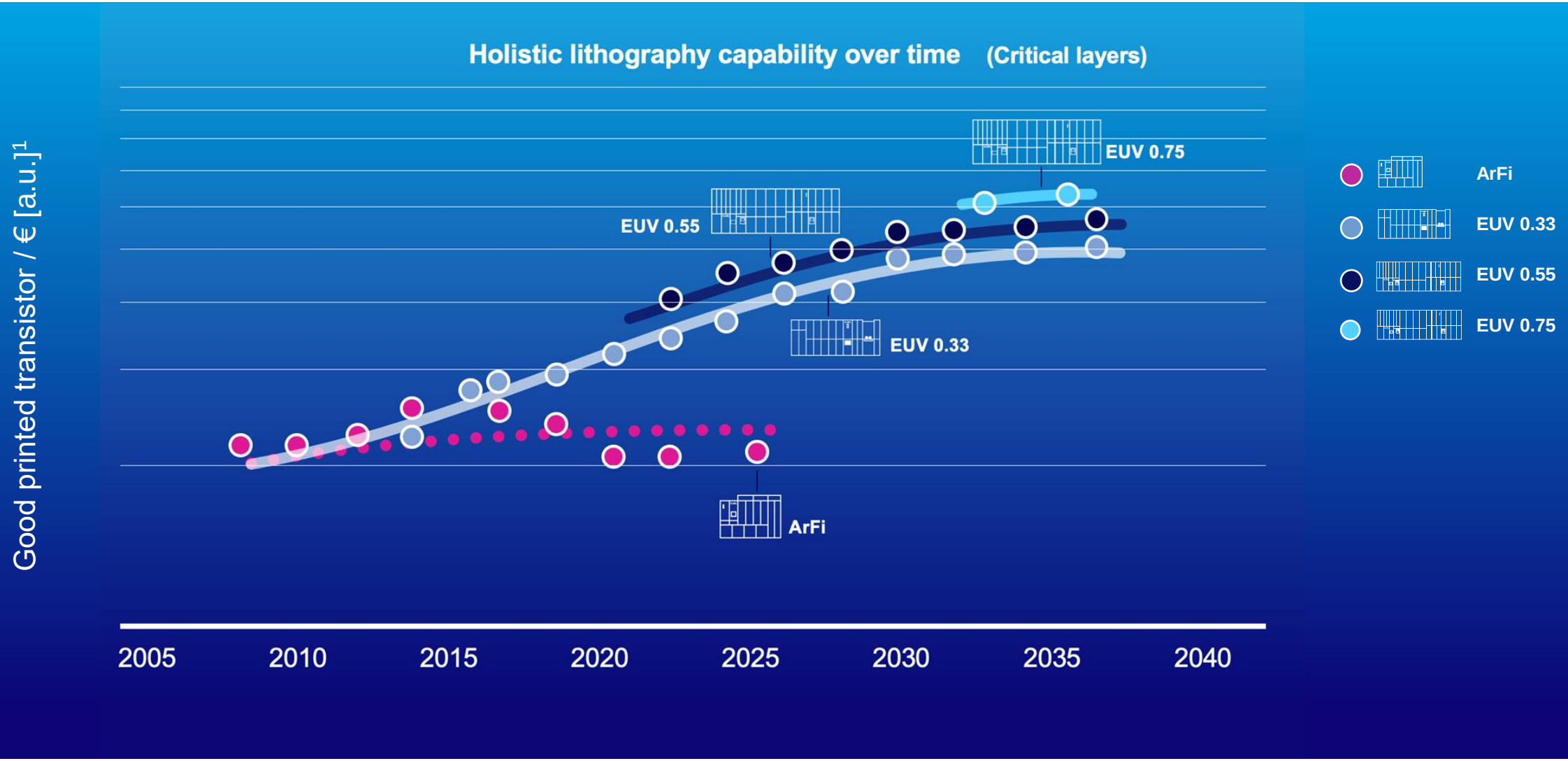


Total cost and emissions of wafer patterning can be reduced by:

1. Increasing the number of good transistor processed at every step
2. Simplifying the overall process flow
3. Minimizing cost and emission of each processing step

ASML has delivered higher transistor density at lower cost for several decades

We believe that EUV scalability & holistic lithography can extend our historical trend into the next decade



[1]Source: ASML, excluding innovations in standard cell design

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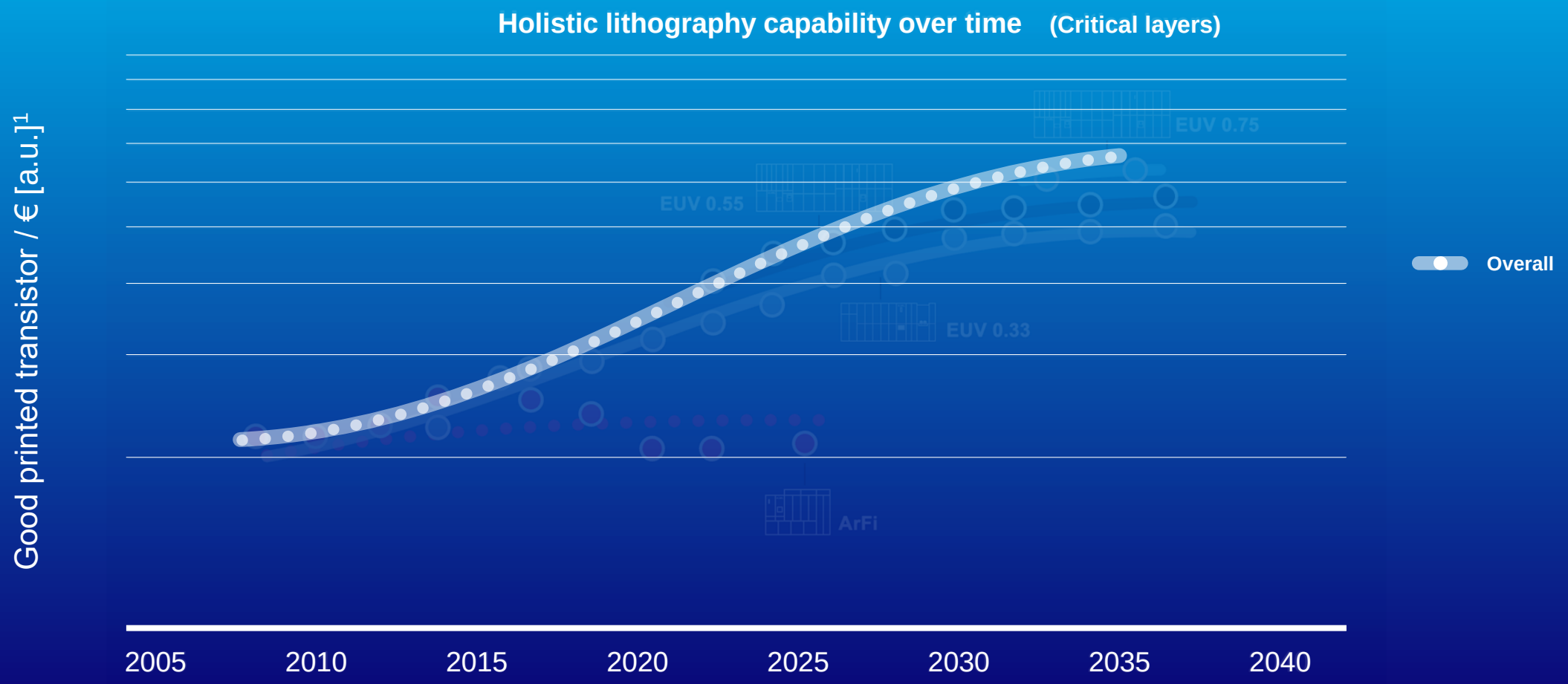
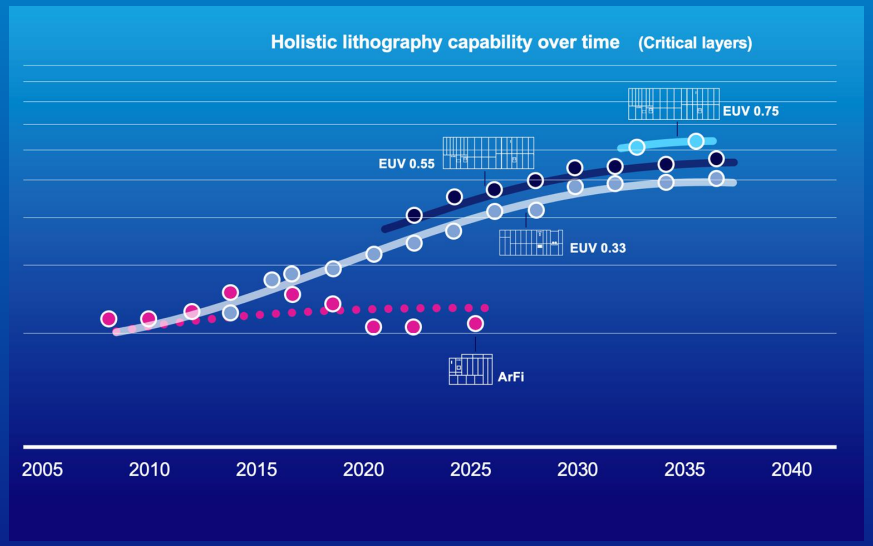


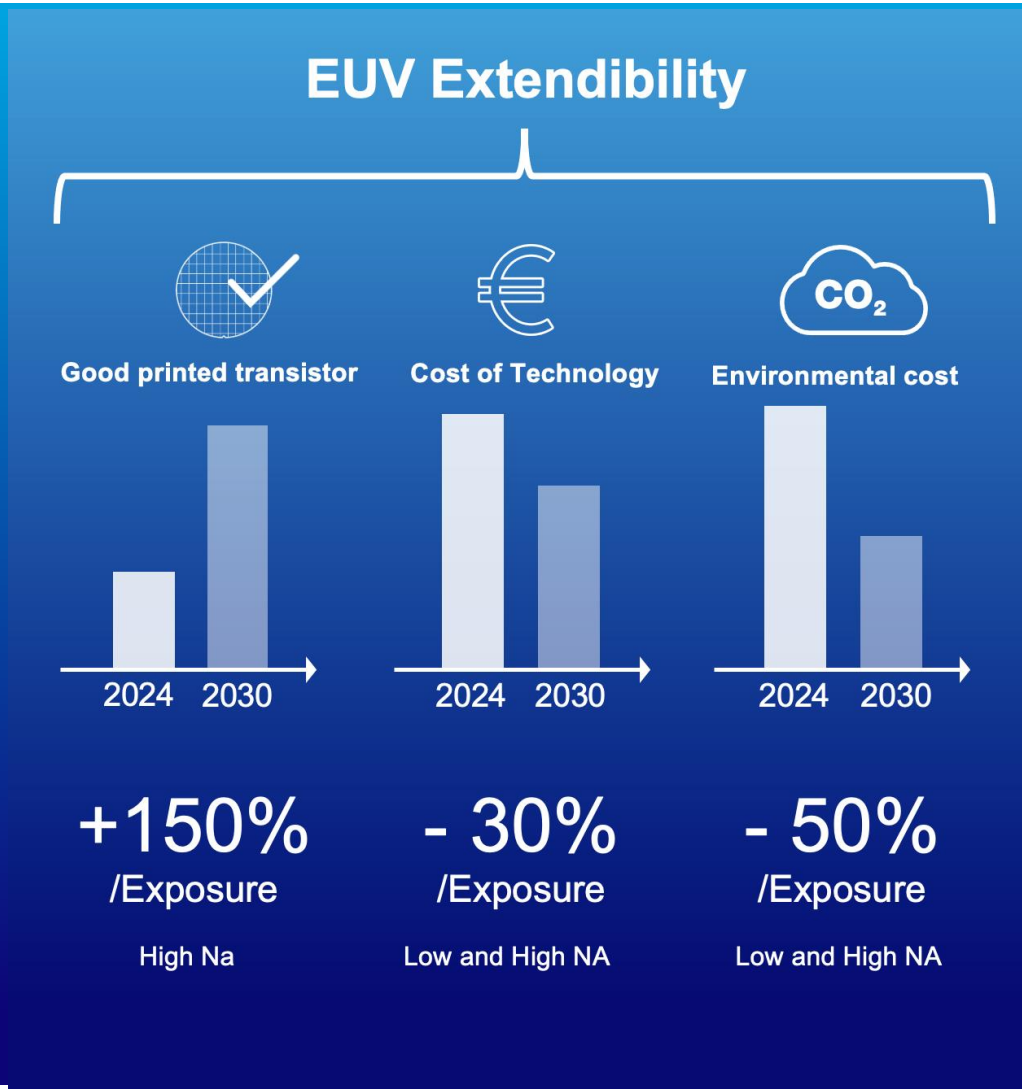
[1]Source: ASML, excluding innovations in standard cell design

ASML's innovations can extend the benefits of EUV lithography

More good transistors at lower cost and energy for customers, at increased profitability for ASML

ASML Holistic lithography value =





Note: Cost / exposure reduction not taking into account possible inflation

ASML's innovations can extend the benefits of EUV lithography

More good transistors at lower cost and energy for customers @ increased profitability for ASML

ASML

Holistic lithography value

=

Good printed transistors

Total lithography cost

ASML intends to innovate on all aspects to maximize its product portfolio value

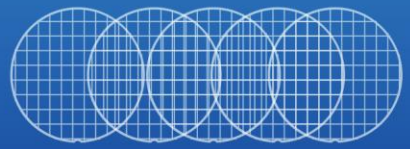
Innovation per product (EUV, DUV…) will target specific customer & market needs

ASML Holistic lithography value =

Good printed transistors

Patterning Yield × Resolution × Accuracy × Productivity

$$CD = k_1 \frac{\lambda}{NA}$$



System cost / Lifetime + Operational cost + Environmental cost

1 Ton CO_2 = 200 EUR

Total lithography cost

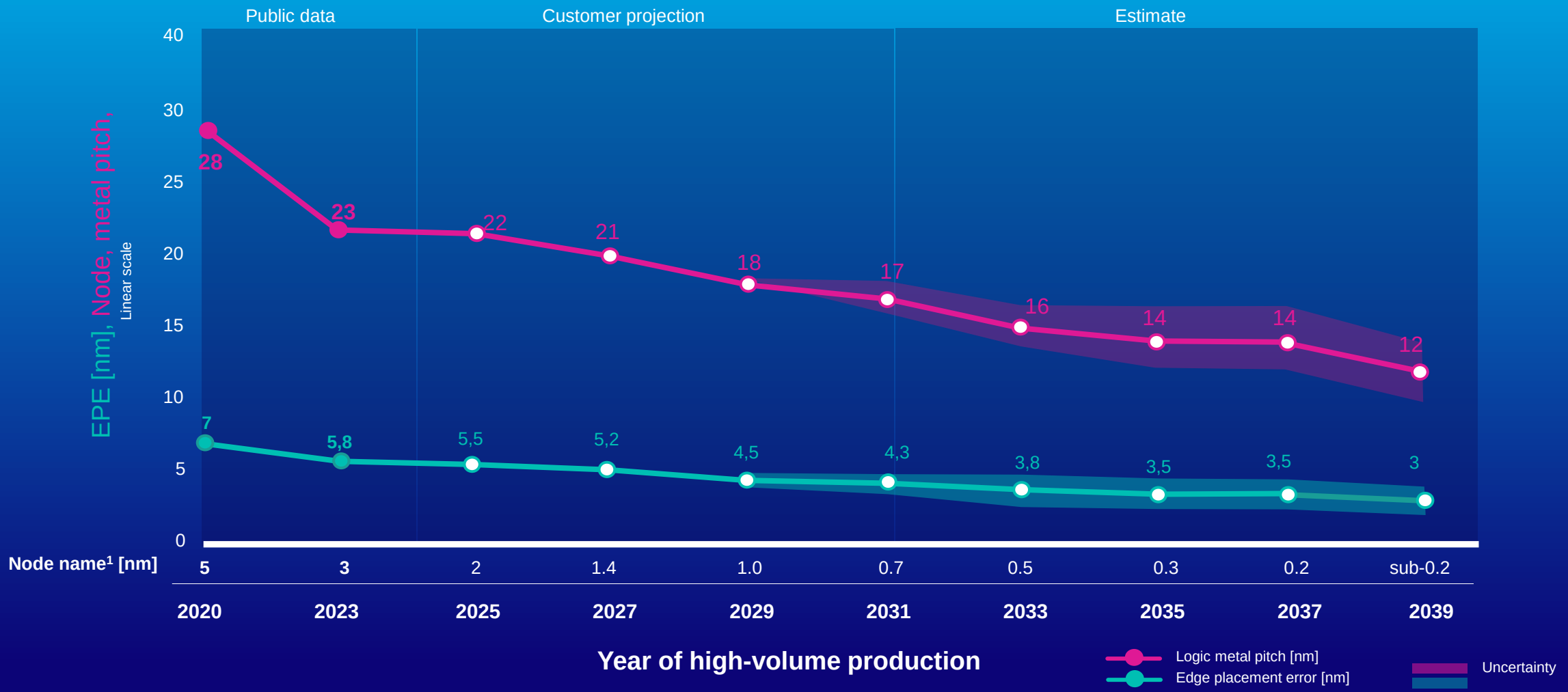
Customer trust and partnership remains at the core of ASML's strategy

We expect that our ability to scale EUV technology into the next decade and extend our versatile holistic lithography portfolio could place ASML at the heart of the AI opportunity. This would continue to create significant growth in revenue and profitability in this decade.

SK hynix **Seon-Yong Cha, SK Hynix CTO**

We anticipate that semiconductor manufacturers will continue to drive shrink

Reducing transistor dimensions likely remains the easiest way to drive density up at reduced cost



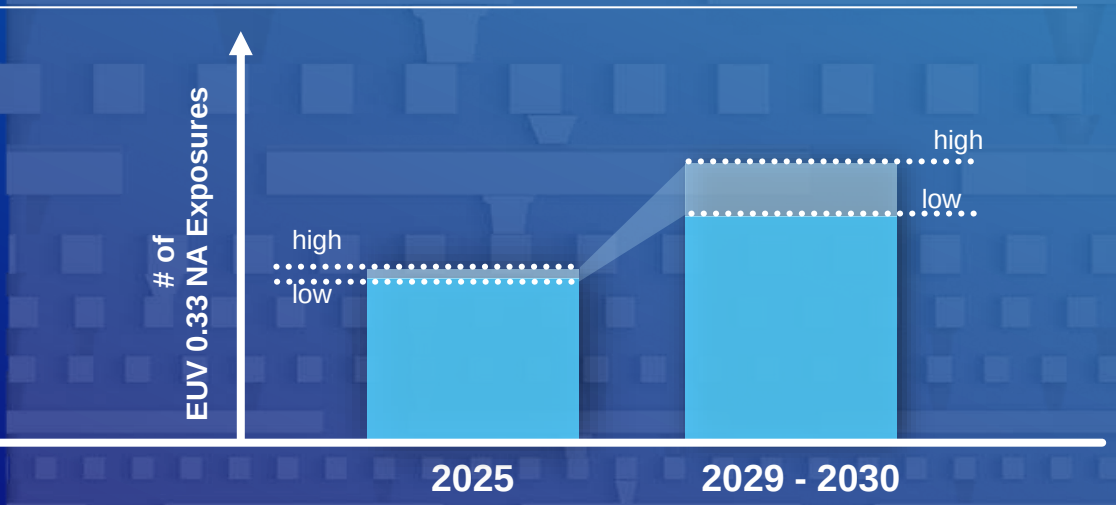
Source: [1]Luc van den Hove, IMEC , ITF May 21, 2024
SP: Single Patterning, DP: Double Patterning, QP: Quadruple Patterning, EPE: Edge Placement Error

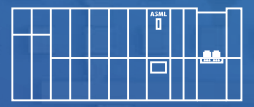
Logic and DRAM are expected to drive further critical lithography exposures

We expect EUV 0.33 NA layers to continue to increase node on node

LOGIC

EUV lithography 0.33NA exposures (weighted average)

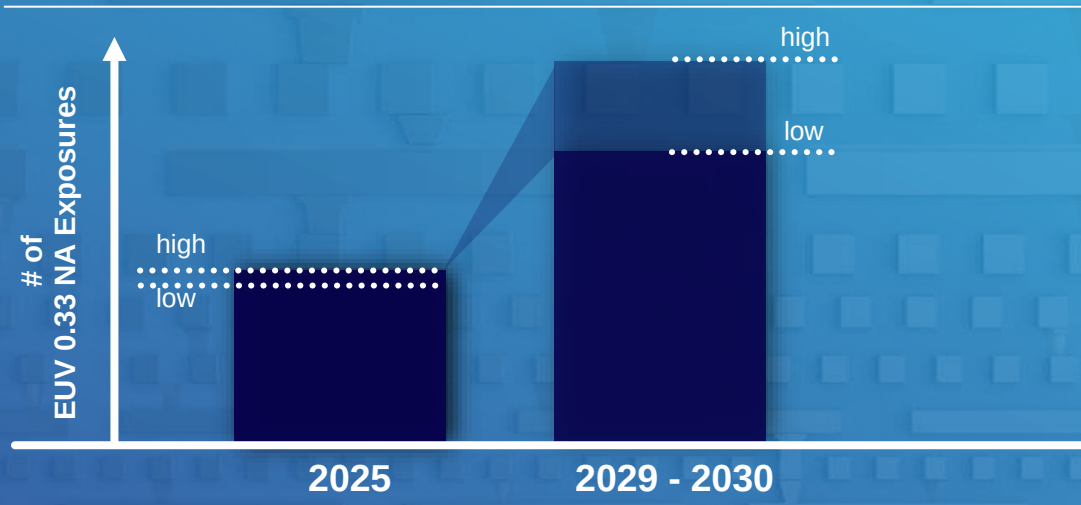




NXE 0.33 NA

DRAM

EUV lithography 0.33NA exposures (weighted average)

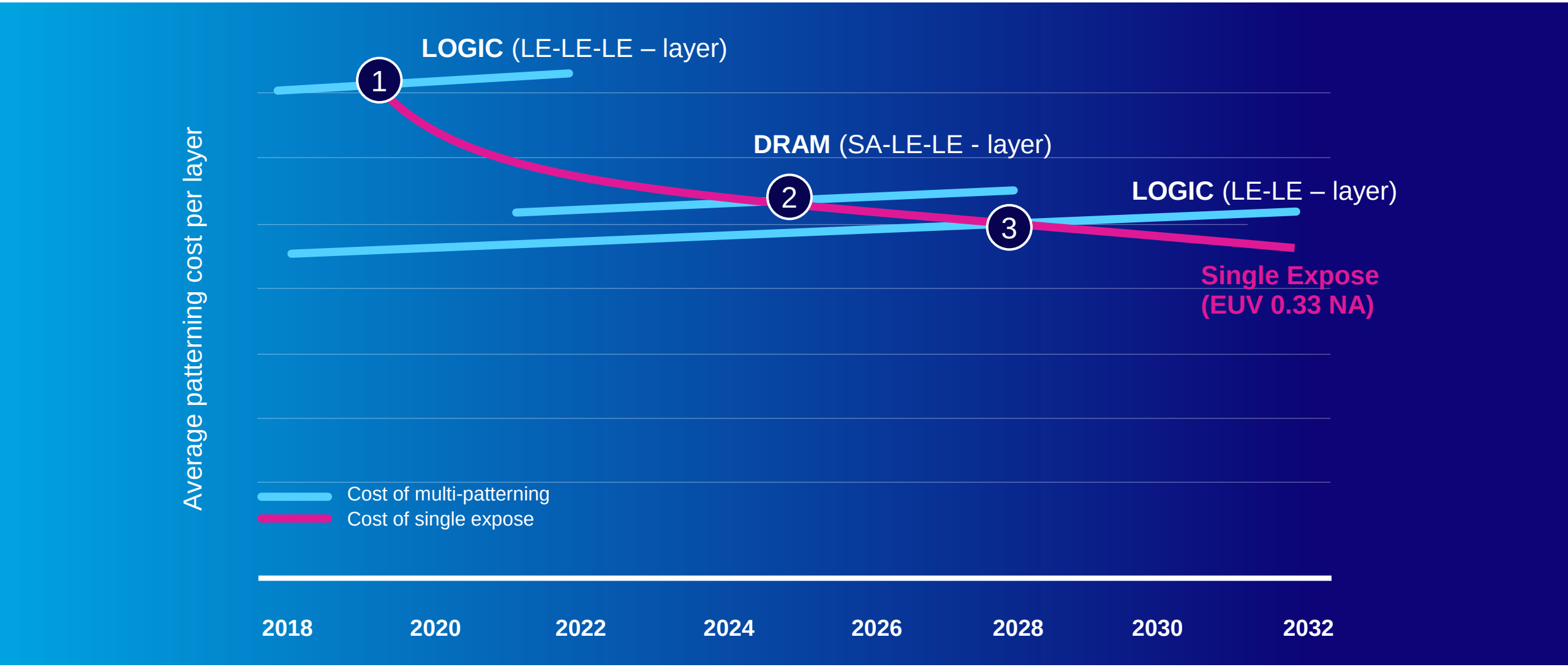


10-20% EUV spend CAGR

15-25% EUV spend CAGR

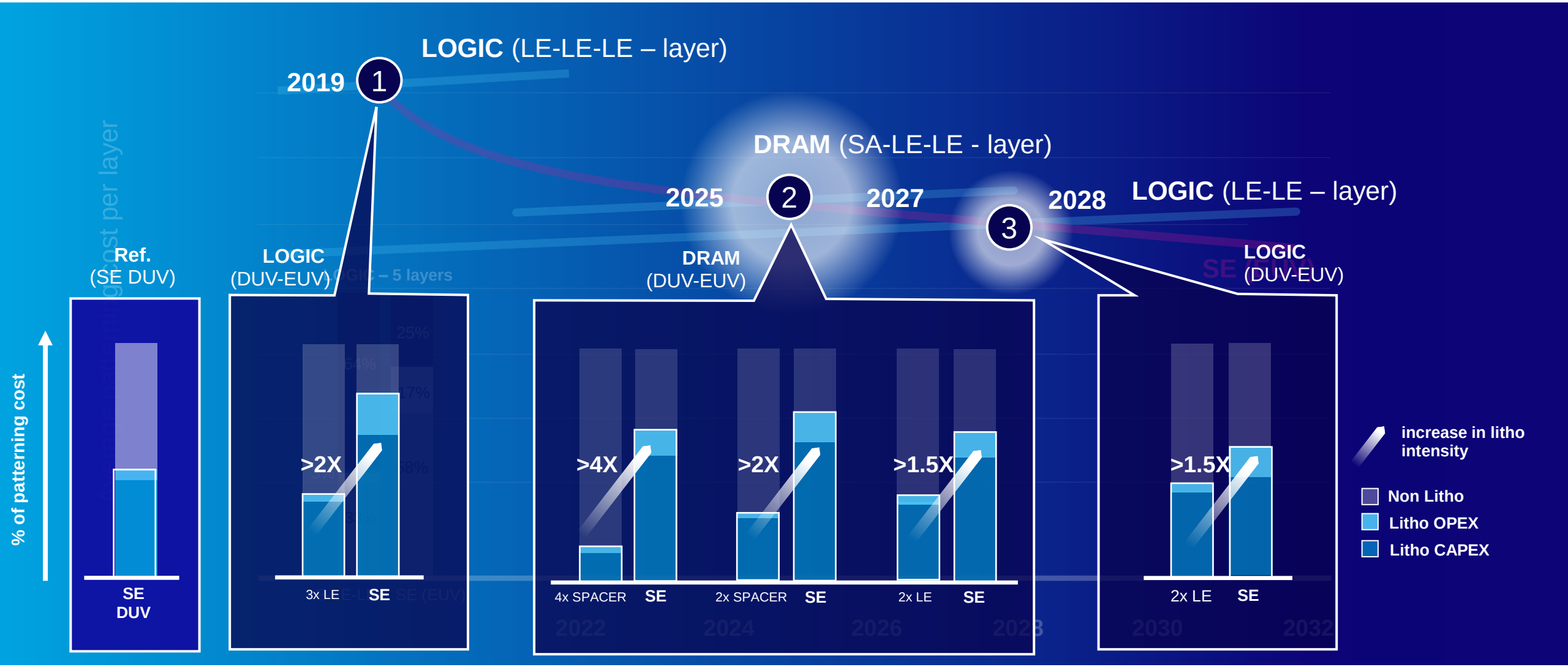
EUV 0.33 NA could enable further multi-patterning to single expose conversion

Resulting in cost, yield and cycle time benefits for our customers

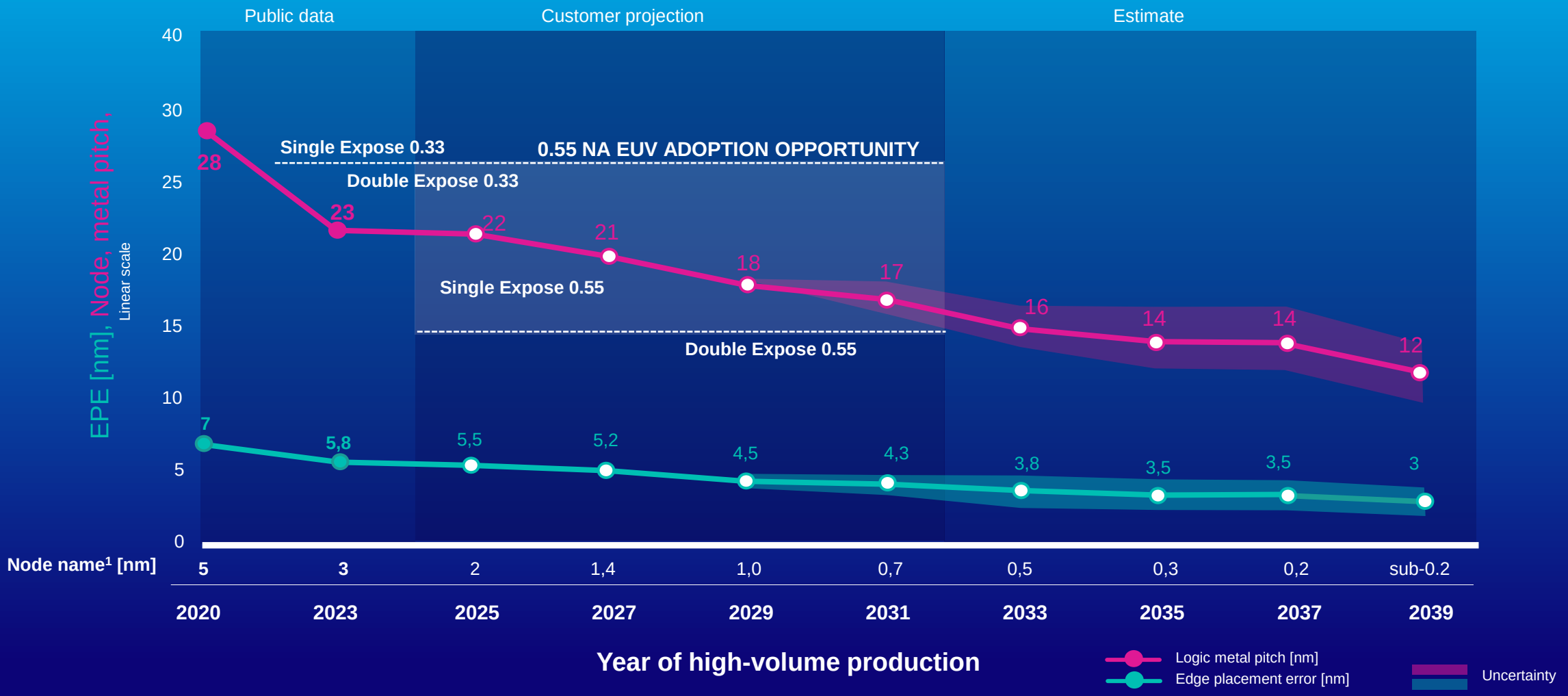


EUV 0.33 NA could enable further multi-patterning to single expose conversion

Resulting in higher number of EUV exposures for ASML between 2025 and 2030



0.55 NA EUV opportunity starts now as 0.33 NA EUV transitions to multi-patterning on <26nm pitch critical layers



Source: [1]Luc van den Hove, IMEC , ITF May 21, 2024
SP: Single Patterning, DP: Double Patterning, QP: Quadruple Patterning

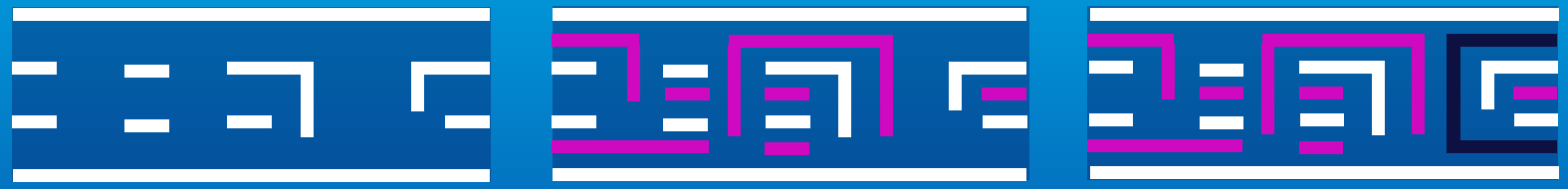
LOGIC: High NA EUV enables more design freedom with 1.5D and 2D designs

Single expose simplification reduces process steps, cycle time and improves yield

Low NA Multi Patterning

P22 in horizontal direction combined with P28 in vertical direction.

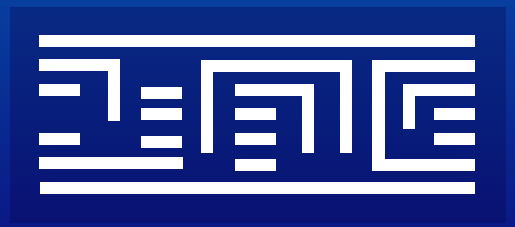
Exposure NXE ① Exposure NXE ② Exposure NXE ③



This multi-exposure method is not performed in high-volume manufacturing due to its complexity.

High NA Single Patterning

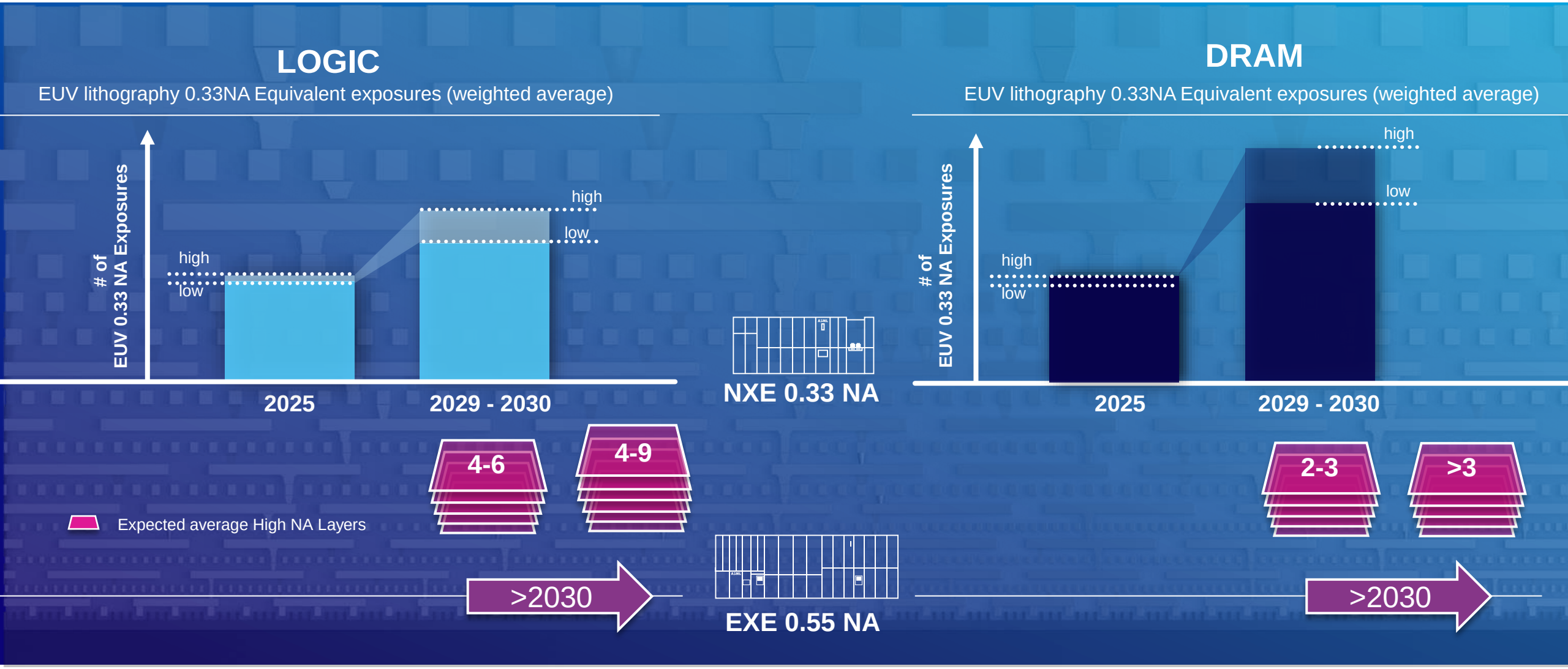
① Exposure High NA



High NA Logic metal: ~35% cost benefit and process simplification

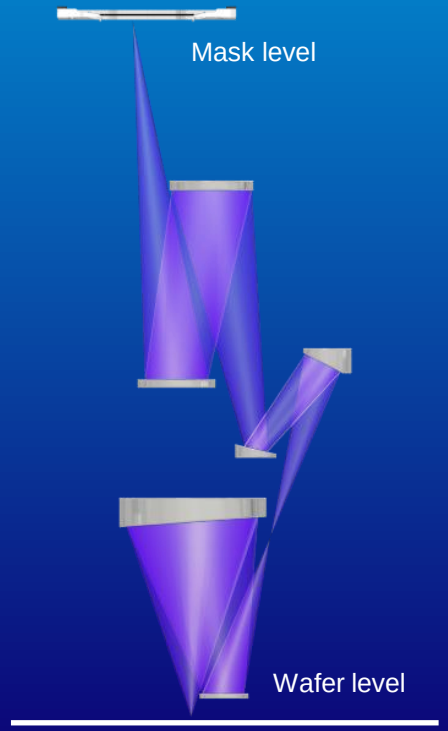
Logic and DRAM are expected to drive further critical lithography exposures

Insertion of High NA in high volume manufacturing in 2026-27, adoption by end of the decade

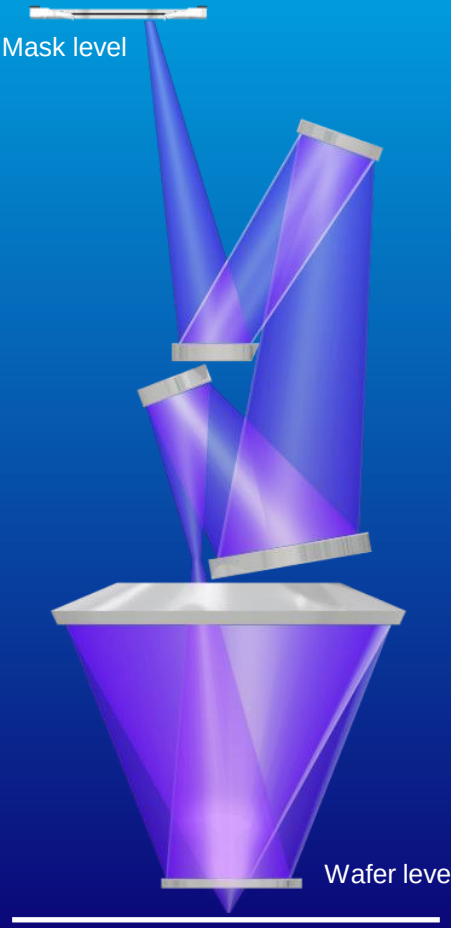


High NA EUV's latest optics innovation sets the base for our EUV roadmap

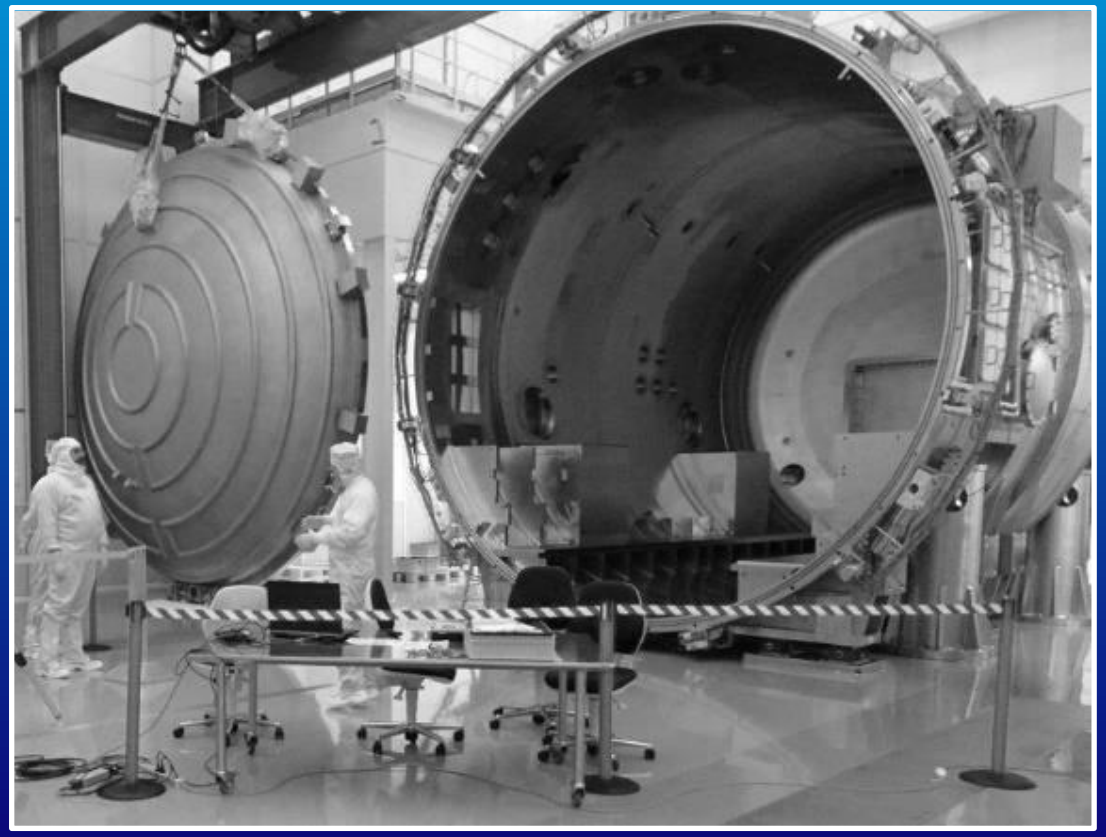
Picometer stability (1/200 Si atom) achieved on aspheric mirrors



NA 0.33



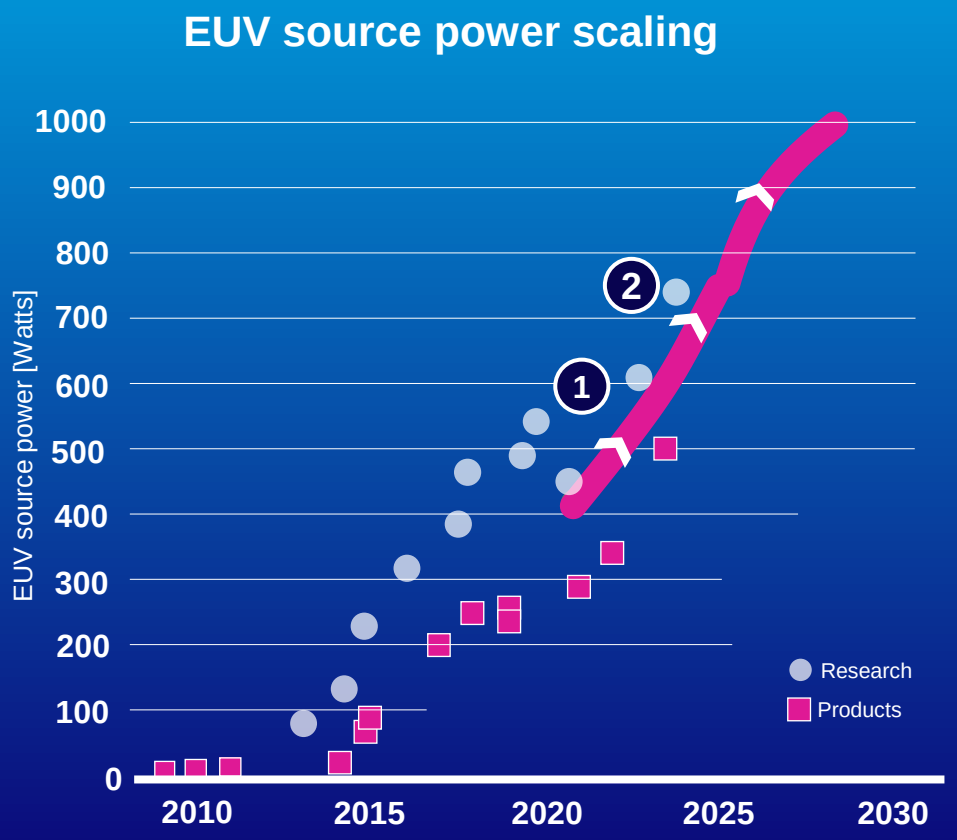
NA >0.5

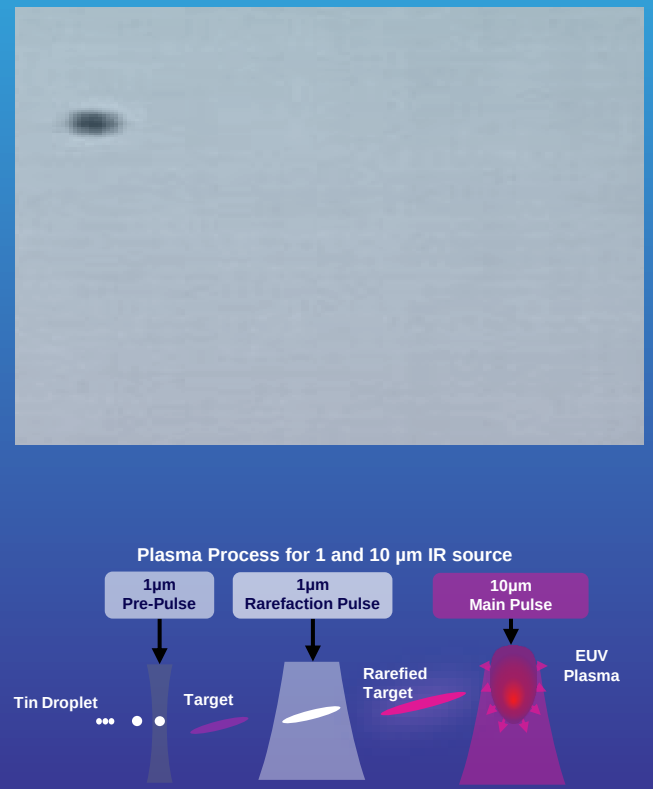


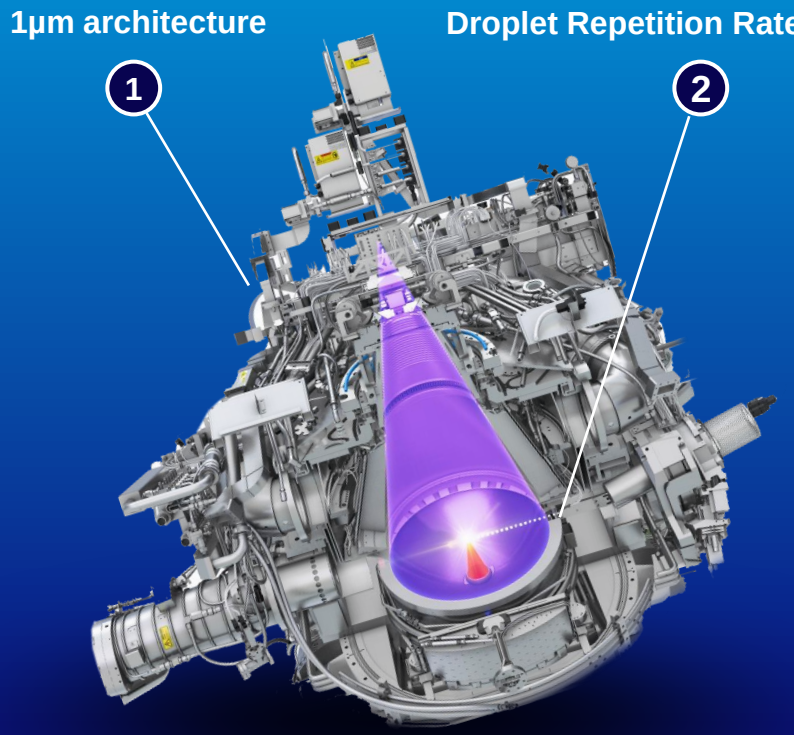
High NA Mirror Metrology at Zeiss

EUV source power continues to scale with opportunity to achieve >1000W

740W EUV power demonstrated - measures identified to reach >1000W in the future







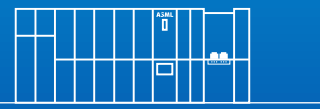
High NA EUV optics support the vision of a higher productivity EUV platform

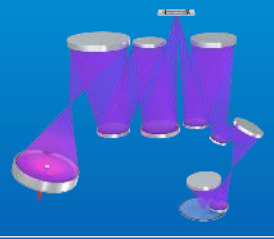
EUV performance and productivity can be extended far into the next decade (>2030)

Today

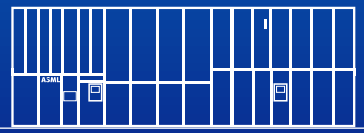
Future: higher productivity platform

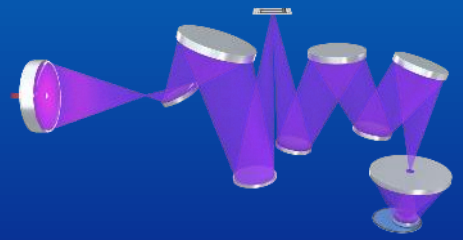
0.33 NA NXE platform



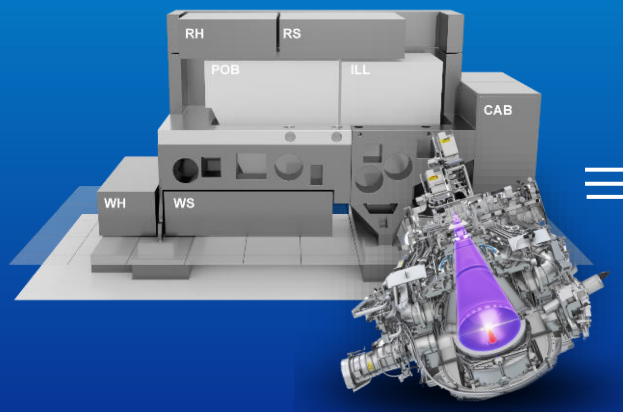


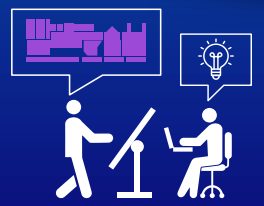
0.55 NA EXE platform

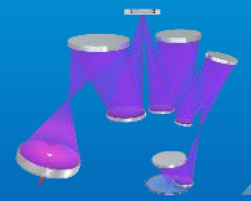


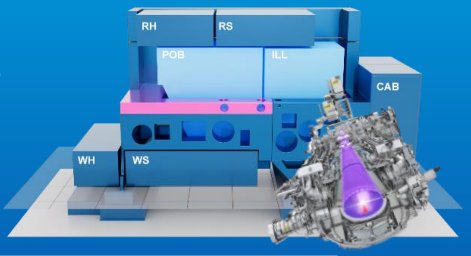


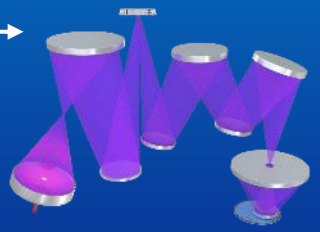
0.75 NA

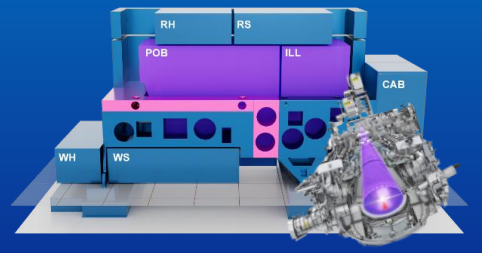


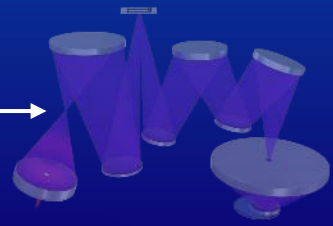


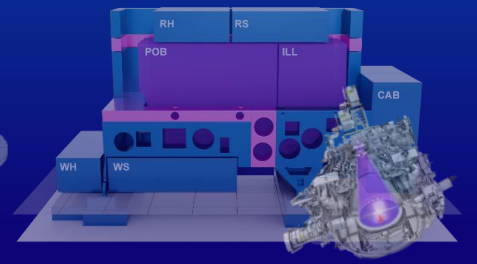








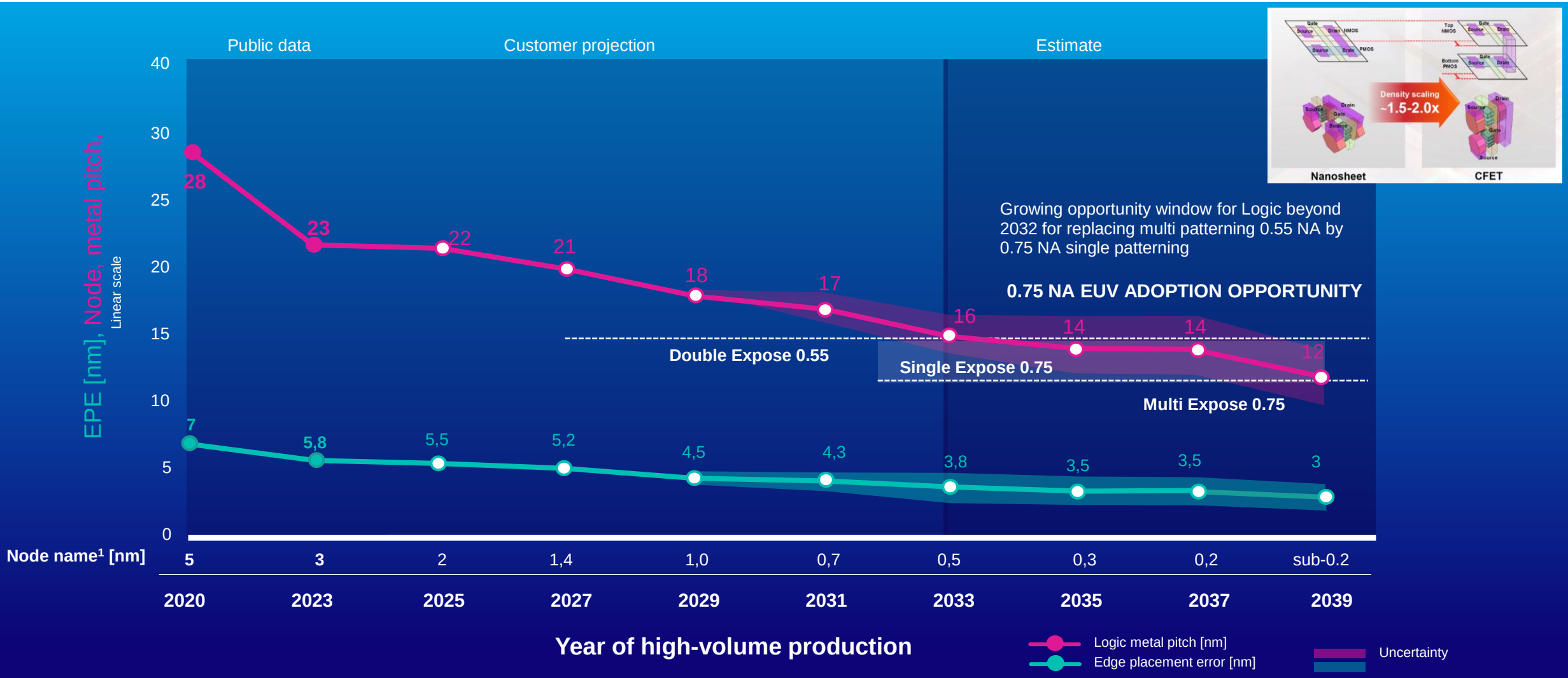




~50% **System commonality** ~95%

0.75 NA EUV opportunity is in the next decade when <16nm pitch will be needed

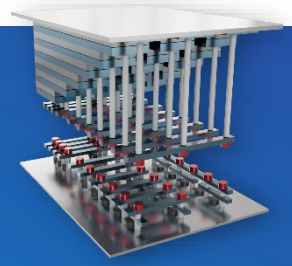
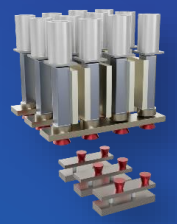
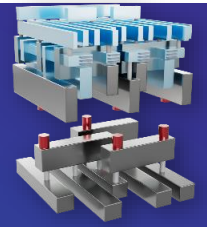
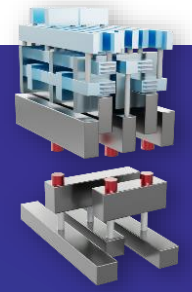
Higher productivity platform can be designed to support future Hyper NA needs



Source: [1]Luc van den Hove, IMEC , ITF May 21, 2024
SP: Single Patterning, DP: Double Patterning, QP: Quadruple Patterning

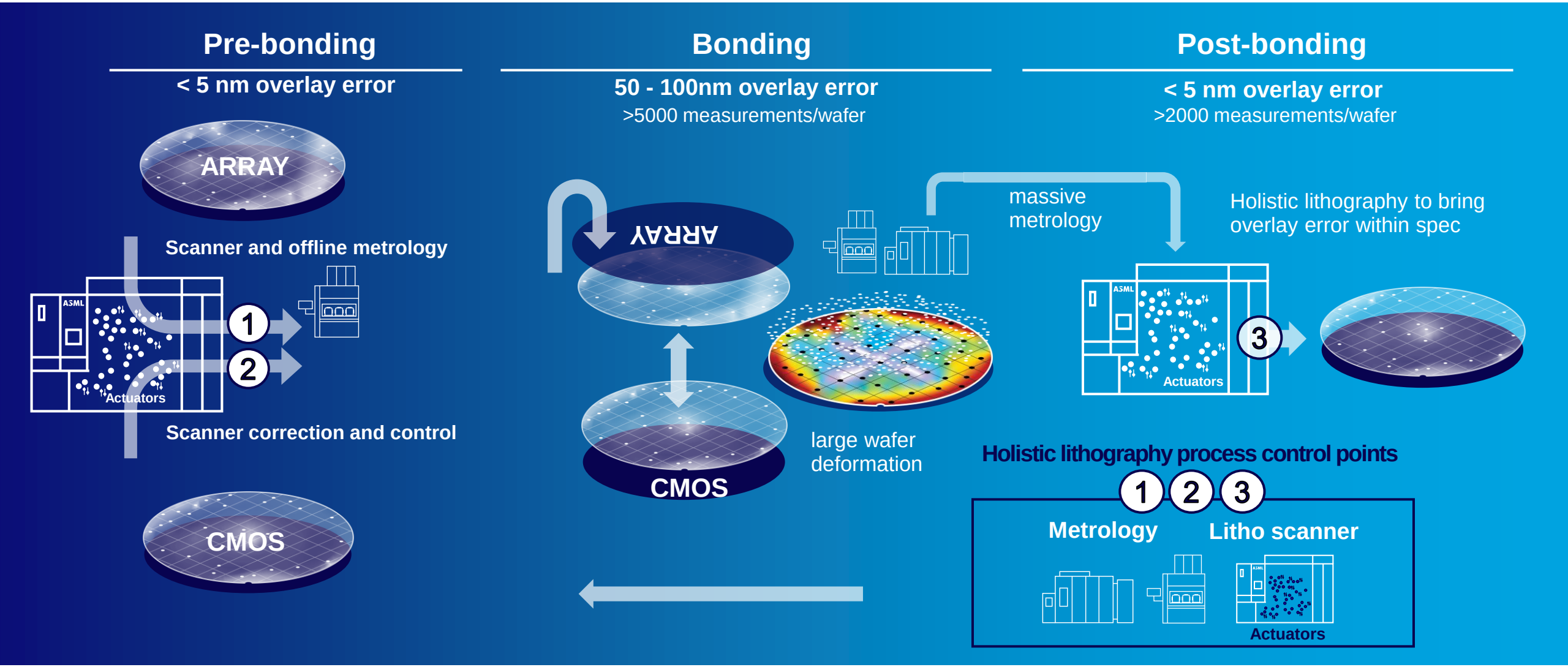
We expect front end 3D integration to complement 2D shrink in driving density

Front end 3D integration challenges will trigger new litho opportunities for all semiconductor products

	NAND		DRAM			LOGIC	
							
	3D NAND		**4F² 2D ARRAY**		**3D ARRAY**	**BSPN**	**CFET**
	HVM	>2030	>2027	>2032	>2032	2026	>2032
Stack	Array + CMOS	Array + Array + CMOS	Array + CMOS	Array + Array + CMOS	Array + CMOS	Logic + Bare-Si	Logic + Logic
Bonding	W-W hybrid	W-W / D-W hybrid	W-W hybrid	W-W / D-W hybrid	W-W hybrid	W-W Fusion	W-W | D-W Fusion
Overlay	**50nm → 25nm**	**50nm → 25nm**	**6nm → 3nm**	**6nm → 3nm**	**>4.5nm**	**2.5nm → 1.6nm**	**5nm → 2nm**
Litho	KrF	KrF	ArFi	ArFi	ArFi	NXE/EXE	NXE/EXE

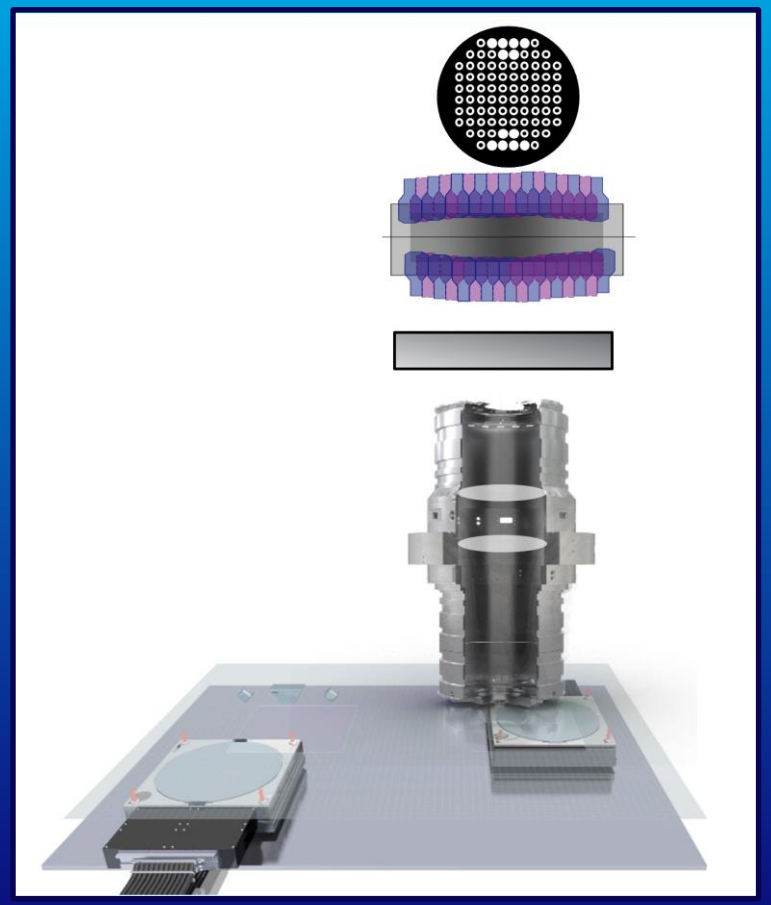
Holistic Lithography should support front end 3D integration

Metrology and scanner control at pre and post bonding are critical process points needed for overlay



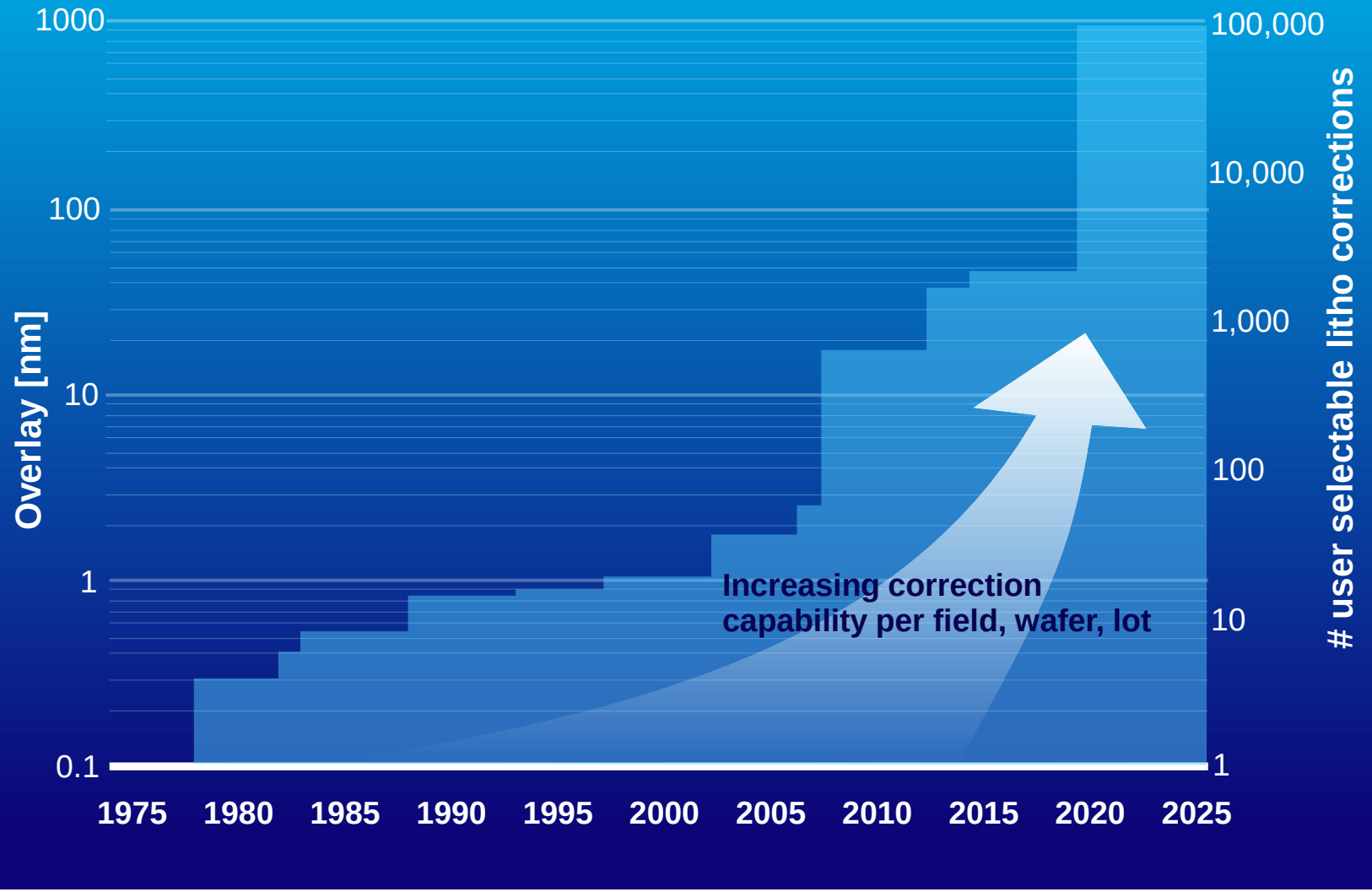
Lithography is a formidable tool to compensate process fingerprints

Correction capability increased ~5 orders of magnitude, now @100 000 parameters per exposure



Metrology stage
100% of wafers are measured

Exposure stage
100% of wafers are processed field-by-field

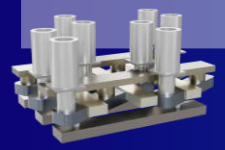


Wafer bonding can drive transistor density increase for DRAM memory

3 scenarios are currently in play for DRAM roadmap, all include bonding and require major innovations

6F²

2025	2026	2027
D1c	D1d	
6F²		



1) CBA: CMOS Bonded Array – CMOS logic wafer bonded to the memory array
2) Stacking: Array bonding – 2 or more memory array wafers bonded to each other. Wafer or die based

Source: Corporate Marketing (CMKT) analysis

Wafer bonding can drive transistor density increase for DRAM memory

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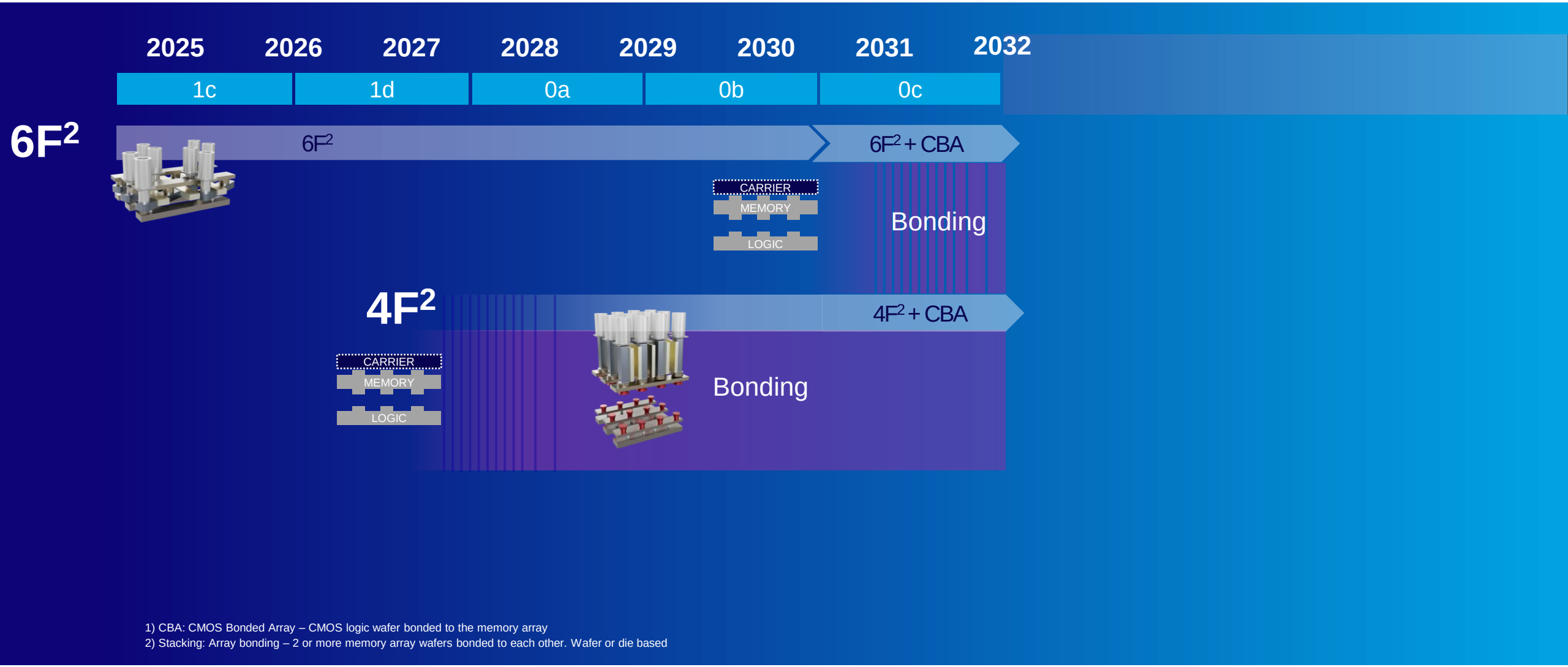

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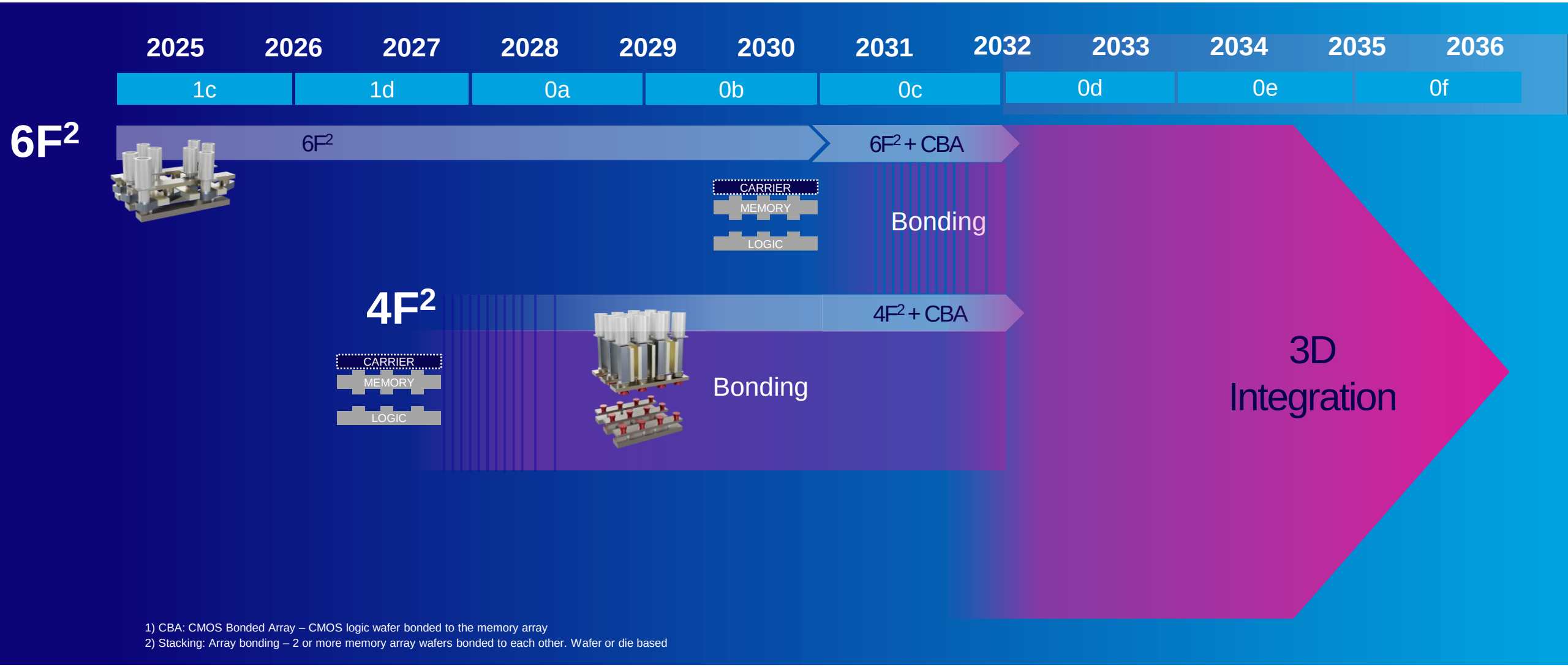

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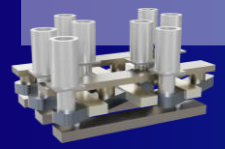
Wafer bonding can drive transistor density increase for DRAM memory

3 scenarios are currently in play for DRAM roadmap, all include bonding and require major innovations

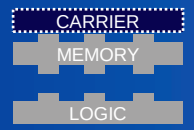
2025 | 2026 | 2027 | 2028 | 2029 | 2030 | 2031 | 2032 | 2033 | 2034 | 2035 | 2036

1c | 1d | 0a | 0b | 0c | 0d | 0e | 0f

$6F^2$



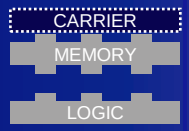
$6F^2$ → $6F^2$ + CBA → **2D Array** $6F^2$ + CBA /Array



Bonding

Bonding + Stacking

$4F^2$

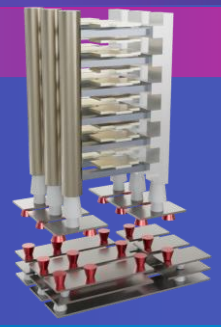


$4F^2$ + CBA → **2D Array** $4F^2$ + CBA /Array

Bonding

Bonding + Stacking

3D Array ~>125 layers



Bonding

1) CBA: CMOS Bonded Array – CMOS logic wafer bonded to the memory array
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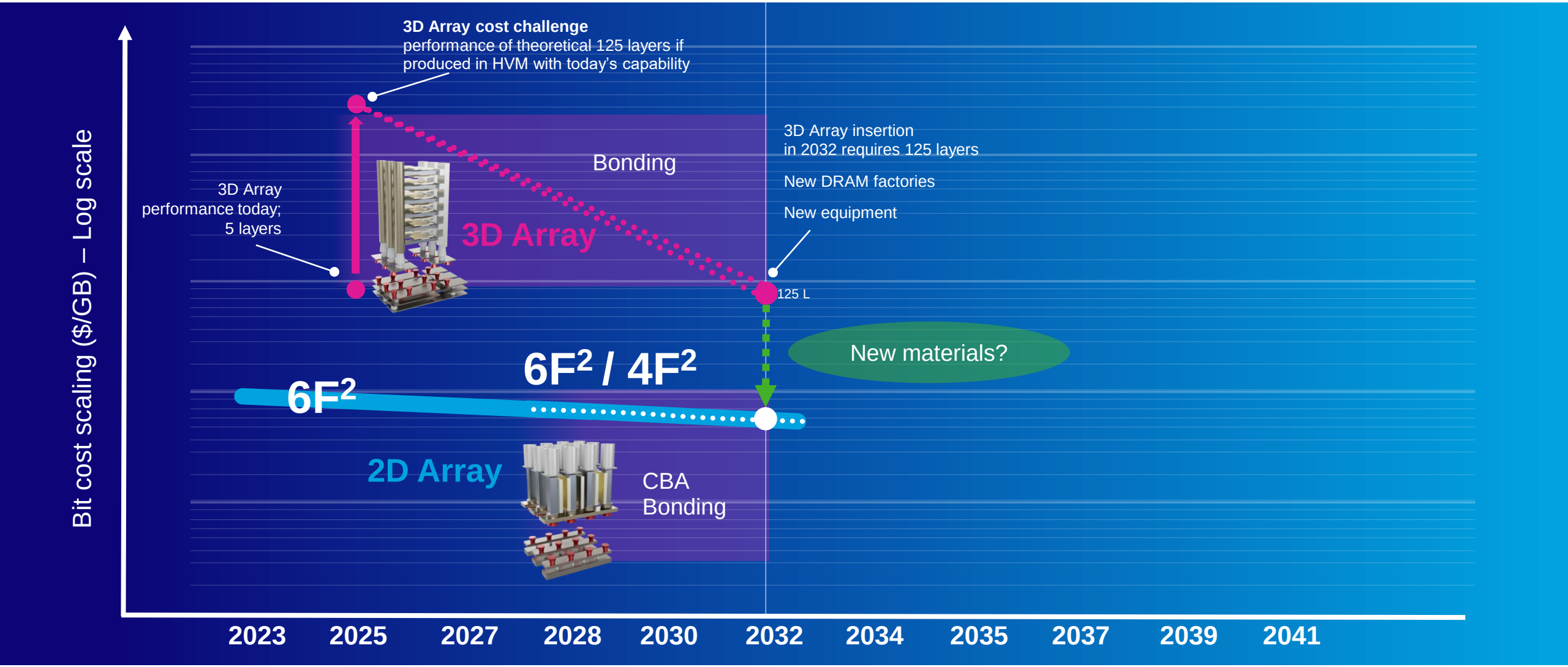
Source: Corporate Marketing (CMKT) analysis

Cost of technology remains a major criteria for our customers' roadmap choices

EUV scalability and holistic lithography can support future front end 3D integration schemes



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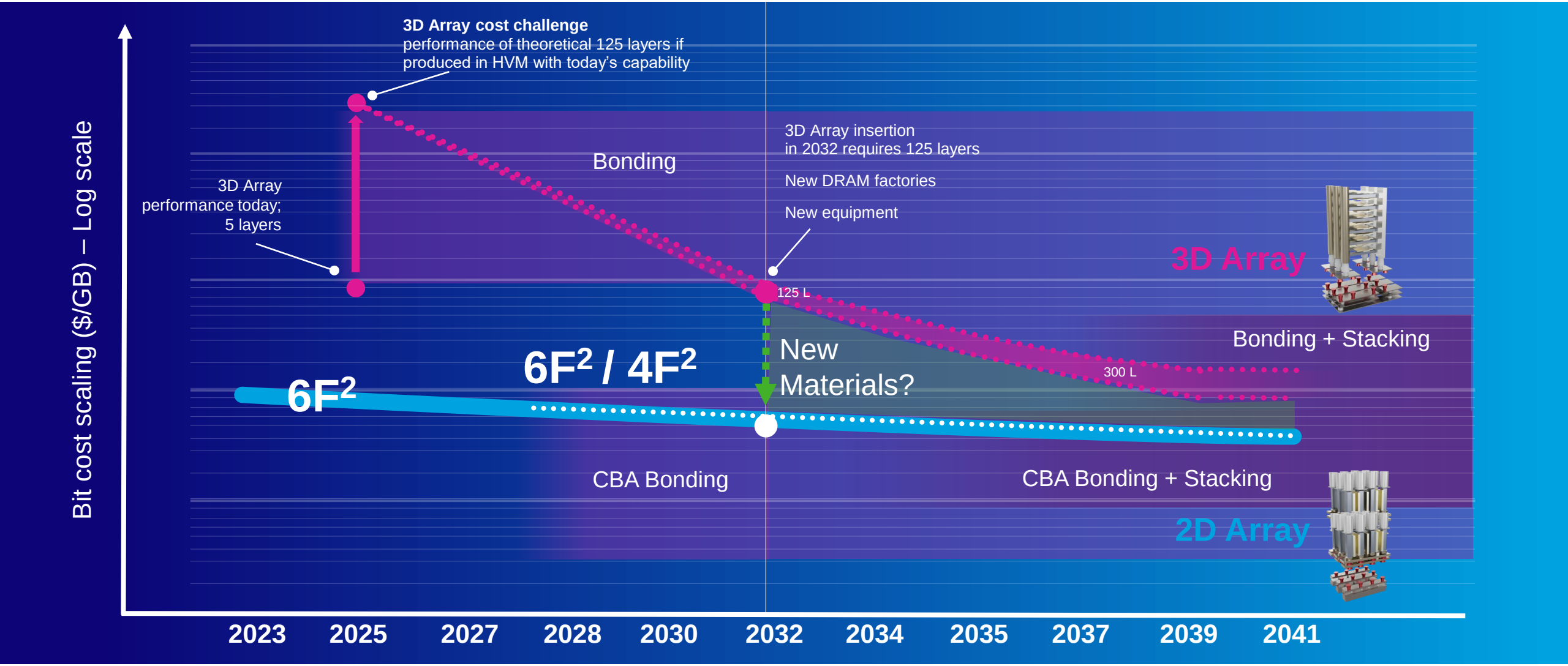
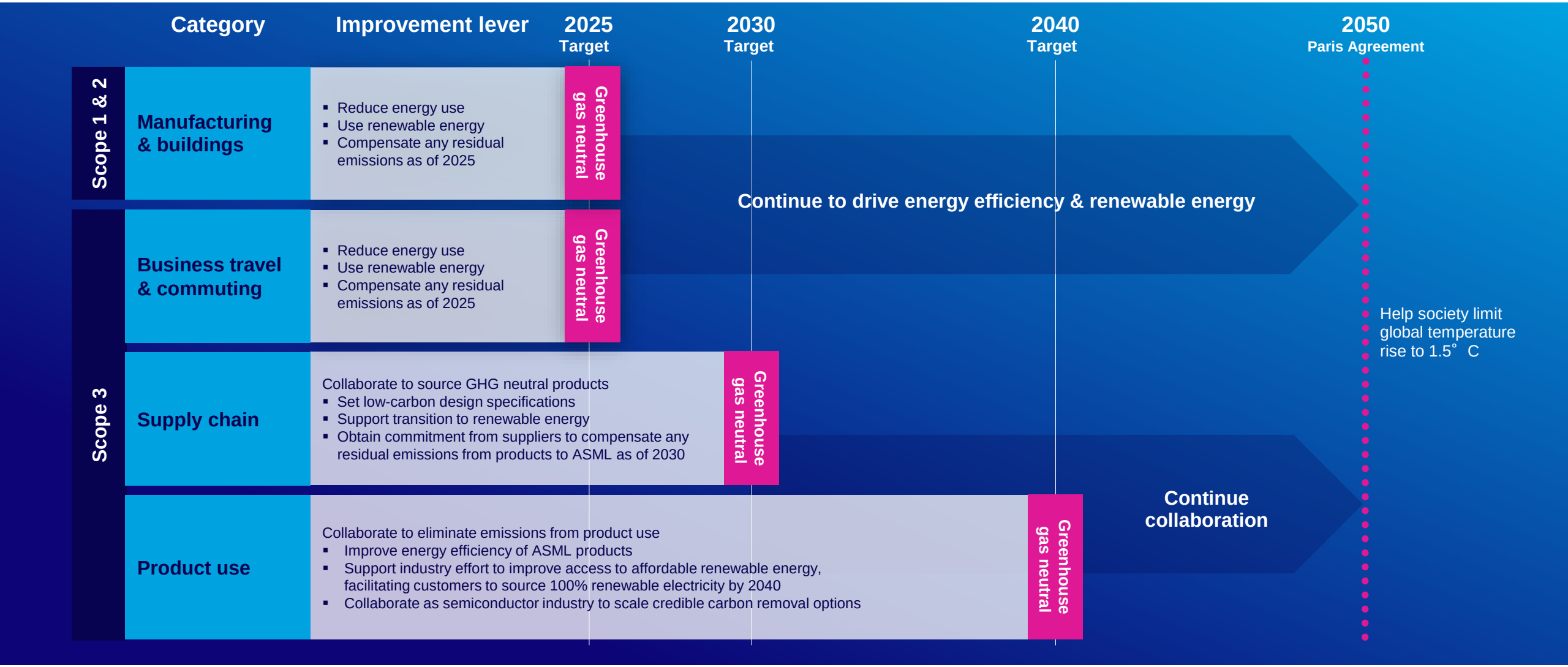


Source: Corporate Marketing (CMKT) analysis

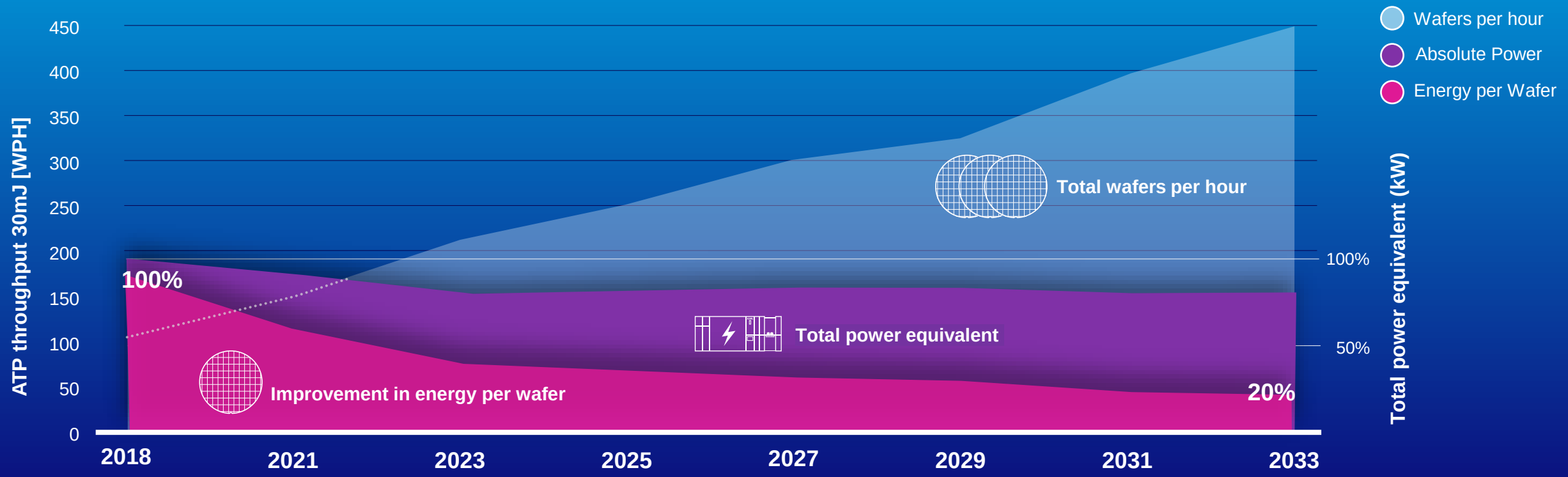
ASML remains committed to its greenhouse gas neutrality ambitions

Intensifying collaboration in the value chain aimed at accelerating climate action



Our EUV innovations are also expected to drive EUV energy consumption down

Within a 15 year period at customers, we anticipate 80% reduction of energy needed per wafer exposed



ASML is increasing its engagement with communities

ASML and communities benefit from each other's presence and support each other's development

Attractive & Inclusive communities

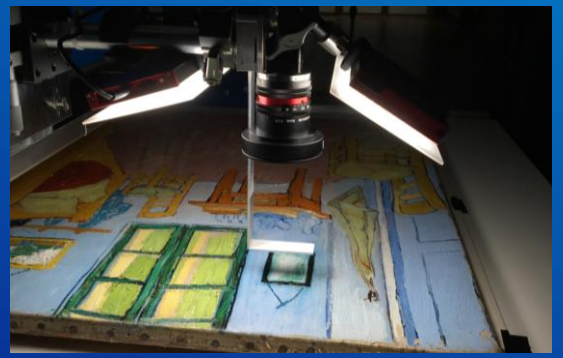
Contribute to positive improvements and experiences in our communities

STEM

Increase the talent pool that society needs to solve some of its key challenges

ESG innovation

Support innovative ideas to solve key ESG challenges



Employee giving

Engage with and care for people in our communities

Forward Looking Statements

This document and related discussions contain statements that are forward-looking within the meaning of the U.S. Private Securities Litigation Reform Act of 1995, including statements with respect to our strategy, plans and expected trends, including trends in end markets and the technology industry and business environment trends, including the emergence of AI and its potential opportunities and expectations for the semiconductor industry, including computing power, advanced logic nodes and DRAM memory, statements with respect to Moore's law and expected transistor growth and aspirations by 2030, global market trends and technology, product and customer roadmaps, long term outlook and expected lithography and semiconductor industry growth and trends and expected growth in semiconductor sales and semiconductor market opportunity through to 2030 and beyond, expected growth in wafer demand and capacity and additional wafer capacity requirements, expected investments by our customers, including investments in our technology and in wafer capacity, plans to increase capacity, expected growth in lithography spend, growth opportunities including opportunities for growth in service and upgrades and opportunities for growth in Installed Base Management sales, expected growth and gross margins in the holistic lithography business and expected addressable market for Applications products, expectations and benefits of a growing installed base, ASML's and its supplier's capacity, expected production of systems, model scenarios and the updated model for 2030, including annual revenue and gross margin opportunity and development potential for 2030, outlook and expected, modelled or potential financial results, including revenue opportunity, gross margin, R&D costs, SG&A costs, capital expenditure, cash conversion cycle and annualized effective tax rate for 2030 and assumptions and drivers underlying such expected, modelled or potential amounts, and other assumptions underlying our business and financial models, expected trends, outlook and growth in semiconductor end markets and long term growth opportunities, demand and demand drivers, expected opportunities and growth drivers for and technological innovation of our products including DUV EUV, High NA, Hyper NA, Applications, and other products impacting productivity and costs, transistor dimensions, logic and DRAM shrink, foundry competition, statements with respect to dividends and share buybacks and our capital return policy, including expectation to return significant amounts of cash to shareholders through growing dividends and buybacks and statements with respect to energy generation and consumption trends and the drive toward energy efficiency, emissions reduction and greenhouse gas neutrality goals and target dates to achieve greenhouse gas neutrality, zero waste from operations and other ESG targets and ambitions and plans to maintain a leadership position in ESG, increasing technological sovereignty across the world and the expected impact on semiconductor sales, including specific goals of countries across the world, increasing competition in the foundry business, estimates for 2024 and other non-historical statements. You can generally identify these statements by the use of words like "may", "will", "could", "should", "project", "believe", "anticipate", "expect", "plan", "estimate", "forecast", "potential", "opportunity", "scenario", "guidance," "intend", "continue", "target", "future", "progress", "goal" and variations of these words or comparable words. These statements are not historical facts, but rather are based on current expectations, estimates, assumptions, models, opportunities and projections about our business and our future and potential financial results and readers should not place undue reliance on them. Forward-looking statements do not guarantee future performance and involve a number of substantial known and unknown risks and uncertainties. These risks and uncertainties include, without limitation, customer demand, semiconductor equipment industry capacity, worldwide demand for semiconductors and semiconductor manufacturing capacity, lithography tool utilization and semiconductor inventory levels, general trends and consumer confidence in the semiconductor industry and end markets, the impact of general economic conditions, including the impact of the current macroeconomic environment on the semiconductor industry, uncertainty around a market recovery including the timing thereof, the impact of inflation, interest rates, wars and geopolitical developments, the impact of pandemics, the performance of our systems, the success of technology advances and the pace of new product development and customer acceptance of and demand for new products, our production capacity and ability to adjust capacity to meet demand, supply chain capacity, timely availability of parts and components, raw materials, critical manufacturing equipment and qualified employees, our ability to produce systems to meet demand, the number and timing of systems ordered, shipped and recognized in revenue, risks relating to fluctuations in net bookings and our ability to convert bookings into sales, the risk of order cancellation or push outs and restrictions on shipments of ordered systems under export controls, risks relating to technology, product and customer roadmaps and Moore's law, risks relating to the trade environment, import/export and national security regulations and orders and their impact on us, including the impact of changes in export regulations and the impact of such regulations on our ability to obtain necessary licenses and to sell our systems and provide services to certain customers, exchange rate fluctuations, changes in tax rates, available liquidity and free cash flow and liquidity requirements, our ability to refinance our indebtedness, available cash and distributable reserves for, and other factors impacting, dividend payments and share repurchases, the number of shares that we repurchase under our share repurchase programs, our ability to enforce patents and protect intellectual property rights and the outcome of intellectual property disputes and litigation, our ability to meet ESG goals and execute our ESG strategy, other factors that may impact ASML's business or financial results including the risk that actual results may differ materially from the models, potential and opportunity we present for 2030 and other future periods, and other risks indicated in the risk factors included in ASML's Annual Report on Form 20-F for the year ended December 31, 2023 and other filings with and submissions to the US Securities and Exchange Commission. These forward-looking statements are made only as of the date of this document. We undertake no obligation to update any forward-looking statements after the date of this report or to conform such statements to actual results or revised expectations, except as required by law.

This document and related discussions contain statements relating to our approach to and interim progress on achieving certain energy efficiency and greenhouse gas emissions reduction targets, including our ambition to achieve greenhouse gas neutrality. References to "greenhouse gas neutral" means remaining emissions, after ASML's efforts to reach its GHG emission reduction targets, compensated by the same amount of metric tons of carbon credits that are verified against recognised quality standards.


THANK
YOU