Public

ODDO TMT Conference – ASML update

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Manager Investor Relations – Europe

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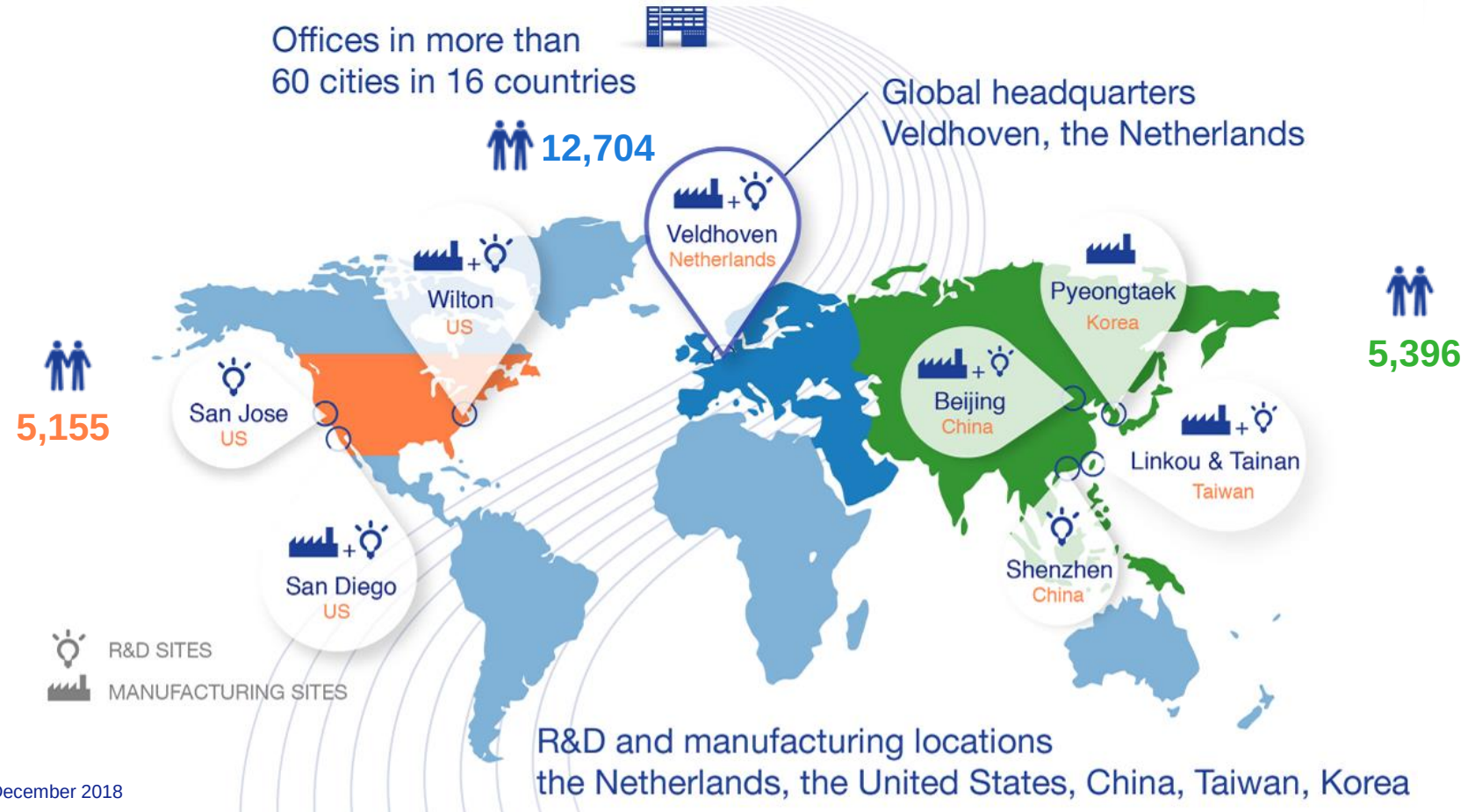
And this happens 50,000 times every second, of every minute, of every hour, of every day…month…year….

Backlight shadowgram from a NXE:3300 EUV source

Forward looking statements

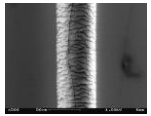
This document contains statements relating to certain projections, business trends and other matters that are forward-looking, including statements with respect to expected trends and outlook, bookings, expected financial results and trends, including expected sales, EUV and DUV revenue, gross margin, R&D and SG&A expenses, and target effective annualized tax rate for the first quarter of 2019, and expected financial results and trends for the full year 2019, including the expectation for continued growth in sales in 2019, with a stronger second half versus the first half, annual revenue opportunity in 2020 and growth potential through 2025, sales and profit targets for 2020, trends in DUV systems revenue and Holistic Lithography and installed based management revenues, expected industry trends and expected trends in the business environment, including continued solid demand for shipments to China, expectations with respect to margins in 2019, including the expected recovery to historic levels by year end statements with respect to the commitment of customers to insert EUV into volume manufacturing by ordering systems, statements with respect to roadmap acceleration, including the introduction of higher productivity systems in 2019 (including the expected shipment of NXE:3400C and expected timing thereof) and the expected benefits, statements with respect to the logic segment expected to be a growth driver, including its expected investment in technology transitions and production capacity for advanced nodes, ASML's commitment to volume manufacturing and secure system performance, shipments, and support for volume manufacturing, including availability, progress supporting EUV ramp and improving consistency, productivity, and production and service capability enabling required volume as planned, including expected shipments (including expected EUV shipments in 2019 and expected availability of chips produced by EUV scanners to customers in 2019), statements with respect to the expected benefits of the introduction of the new DUV system and expected demand for such system, the expected benefits of the introduction of technologies from ASML's Brion and HMI product groups, the expected benefits of the new options for the TWINSCAN XT:860M KrF scanner and of the Advanced Wafer Clamping System (AWACS), the expected negative impact of the fire at one of ASML's suppliers on sales, including the expected recovery timeline, shrink being a key industry driver supporting innovation and providing long-term industry growth, technology innovation driving growth in the next years, Holistic Lithography enabling affordable shrink and delivering value to customers, DUV, EUV and Application products providing unique value drivers for ASML and its customers, the expected continuation of Moore's law and that EUV will continue to enable Moore's law and drive long term value for ASML well into the next decade, the intention to continue to return excess cash to shareholders through growing dividends and regularly timed share buybacks in line with ASML's policy, statements with respect to the proposed dividend for the 2019 Annual General Meeting of Shareholders and the share repurchase plan for 2018-2019, including the intention to use certain shares to cover employee share plans and cancel the rest of the shares upon repurchase, and statements with respect to the expected impact of accounting standards. You can generally identify these statements by the use of words like "may", "will", "could", "should", "project", "believe", "anticipate", "expect", "plan", "estimate", "forecast", "potential", "intend", "continue", "targets", "commits to secure" and variations of these words or comparable words. These statements are not historical facts, but rather are based on current expectations, estimates, assumptions and projections about the business and our future financial results and readers should not place undue reliance on them. Forward-looking statements do not guarantee future performance and involve risks and uncertainties. These risks and uncertainties include, without limitation, economic conditions, product demand and semiconductor equipment industry capacity, worldwide demand and manufacturing capacity utilization for semiconductors, including the impact of general economic conditions on consumer confidence and demand for our customers' products, competitive products and pricing, the impact of any manufacturing efficiencies and capacity constraints, performance of our systems, the continuing success of technology advances and the related pace of new product development and customer acceptance of and demand for new products including EUV and DUV, the number and timing of EUV and DUV systems shipped and recognized in revenue, timing of EUV orders and the risk of order cancellation or push out, EUV production capacity, delays in EUV systems production and development and volume production by customers, including meeting development requirements for volume production, demand for EUV systems being sufficient to result in utilization of EUV facilities in which ASML has made significant investments, potential inability to recover as planned or at all from the negative sales impact of the fire at one of our suppliers, potential inability to successfully integrate acquired businesses to create value for our customers, our ability to enforce patents and protect intellectual property rights, the outcome of intellectual property litigation, availability of raw materials, critical manufacturing equipment and qualified employees, trade environment, changes in exchange rates, changes in tax rates, available cash and liquidity, our ability to refinance our indebtedness, distributable reserves for dividend payments and share repurchases, results of the share repurchase plan and other risks indicated in the risk factors included in ASML's Annual Report on Form 20-F and other filings with the US Securities and Exchange Commission. These forward-looking statements are made only as of the date of this document. We do not undertake to update or revise the forward-looking statements, whether as a result of new information, future events or otherwise.

Employees, R&D and manufacturing locations

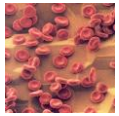


ASML enables Moore's law by providing lithography equipment to produce smaller and more powerful chips

A chip up close



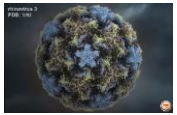
Hair: 50.000nm
Growth: 8nm/sec



Red bloodcell:
7,500nm

Bacteria: 800
to 1,000nm

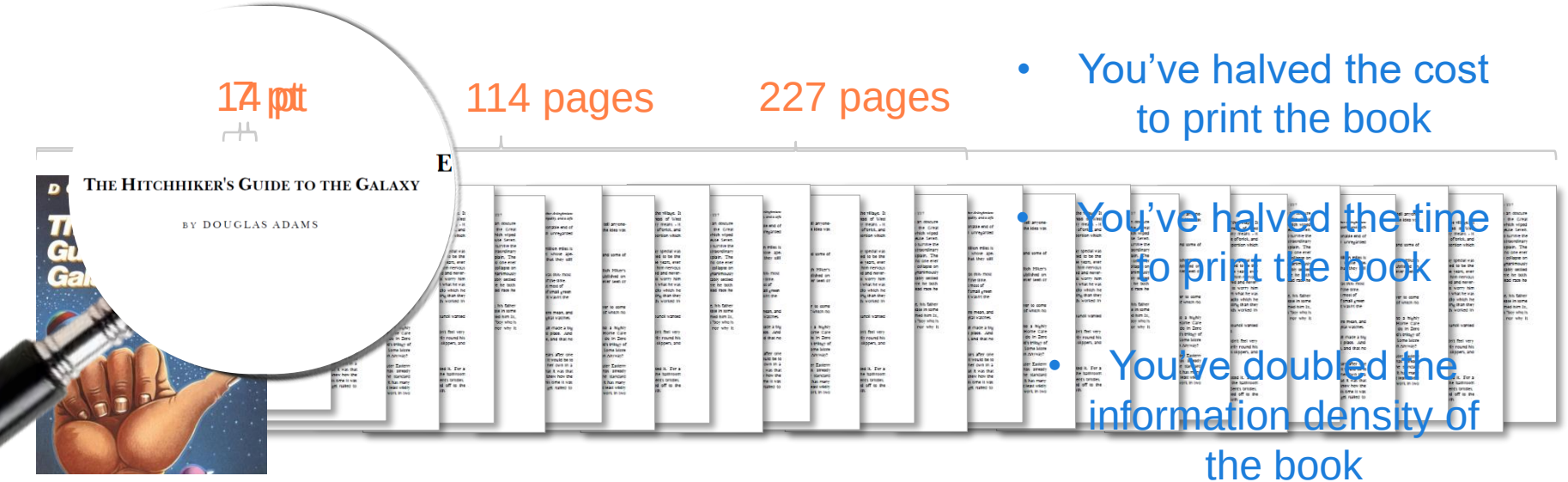
Gras growth:
33nm/sec



Common cold
virus: 30nm

Moore’s Law is a law of economics

- Imagine printing the book The Hitchhiker’s Guide To The Galaxy (by the late great Douglas Adams)
- That’s 227 pages at font size 14
- Now shrink all text to font size 7 and observe Moore’s Law at work



- You’ve halved the cost to print the book
- You’ve halved the time to print the book
- You’ve doubled the information density of the book

ASML enables Logic process evolution

ASML

Public

2007
iPhone

2009
iPhone 3G

2010
iPhone 4

2011
iPhone 4S

2012
iPhone 5

2013
iPhone 5S

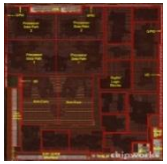
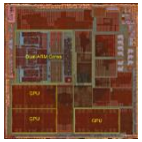
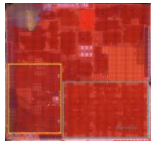
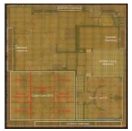
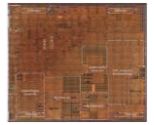
2014
iPhone 6(+)

2015
iPhone 6S(+)

2016
iPhone 7 (+)
(dual lens design)

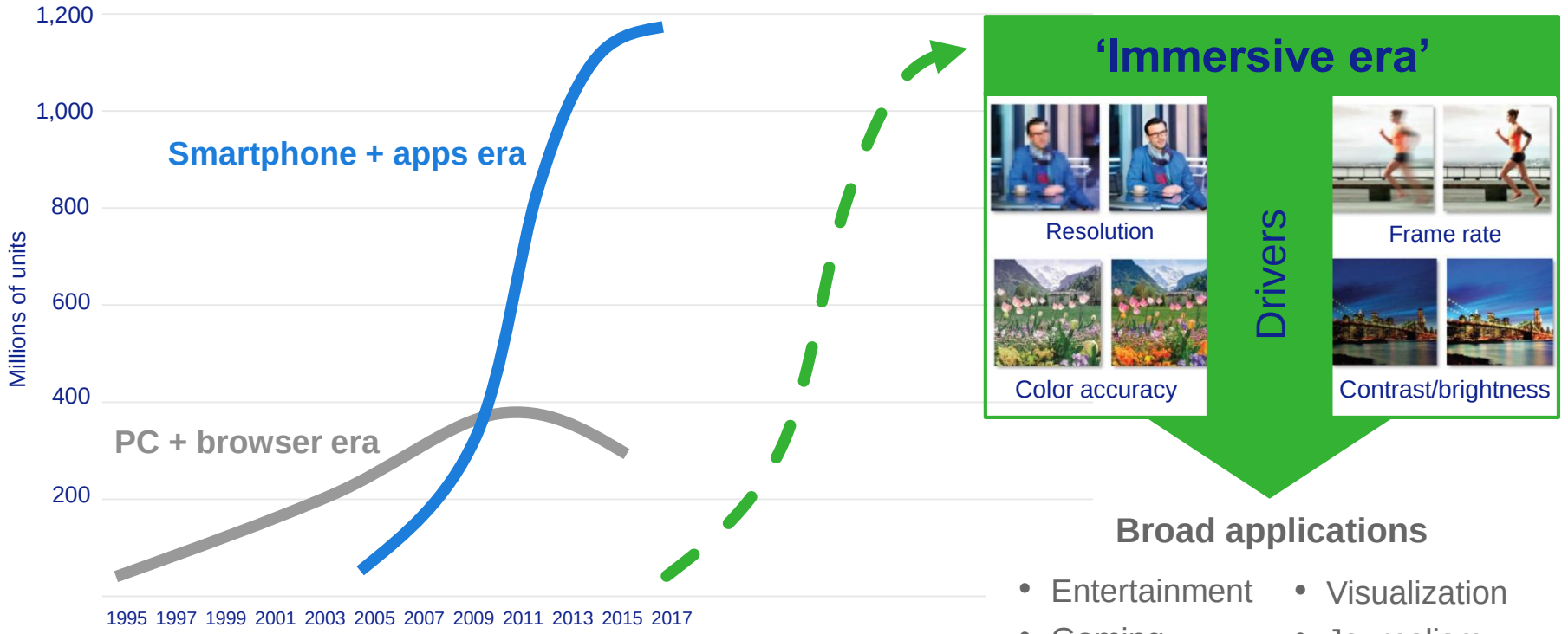
2017
iPhone
8,8+,X

2018
iPhone
XS,XR

APL0098	APL2298	A4	A5	A6	A7	A8	A9	A10	A11	A12
90nm	**65nm**	**45nm**		**32nm**	**28nm**	**20nm**	**14/16nm**	**16nm+**	**10nm**	**7nm**
XT:12X0 Shrink Add functions	*XT:14X0 Shrink Add functions*	*XT:17X0I Shrink Add functions*	*Add functions*	*XT:19X0I Shrink Add functions*	*NXT:1950Ai Shrink Add functions*	*NXT:1960Bi Shrink Add functions*	*NXT:1970Ci Shrink Add functions*	*Add functions*	*NXT:1980Di Shrink Add functions*	*NXT:1980Di Shrink Add functions*
72mm²	**71.8mm²**	**53.3mm²**	**122.2mm²**	**97mm²**	**102mm²**	**87.4mm²**	**96-104mm²**	**125mm²**	**89mm²**	**83mm²**
										
16 bit 1 Core 1 GPU 412 MHz	32 bit 1 Core 1 GPU 412 MHz	32 bit 1 Core 1 GPU 0.8 GHz	32 bit 2 Core 2 GPU 0.8 GHz	32 bit 2 Core 3 GPU 1.2 GHz	64 bit 2 Core 4 GPU 1.3 GHz	64 bit 2 Core 4 GPU 1.4 GHz	64 bit 2 Core 6 GPU 1.85 GHz L14&N16FF	64 bit 4 Core 6 GPU 2.37 GHz **N16FF+ InFO** wafer-level pckg	4.3B transistors 2 +4 Core CPU (4 + 1)GPU + NPU 2.4 GHz **N10FF**	6.9B transistors 2 +4 Core CPU (6)GPU +8 NPU 2.5 GHz **N7FF**

Source: ASML Market Research

Immersive devices will be the next computing wave

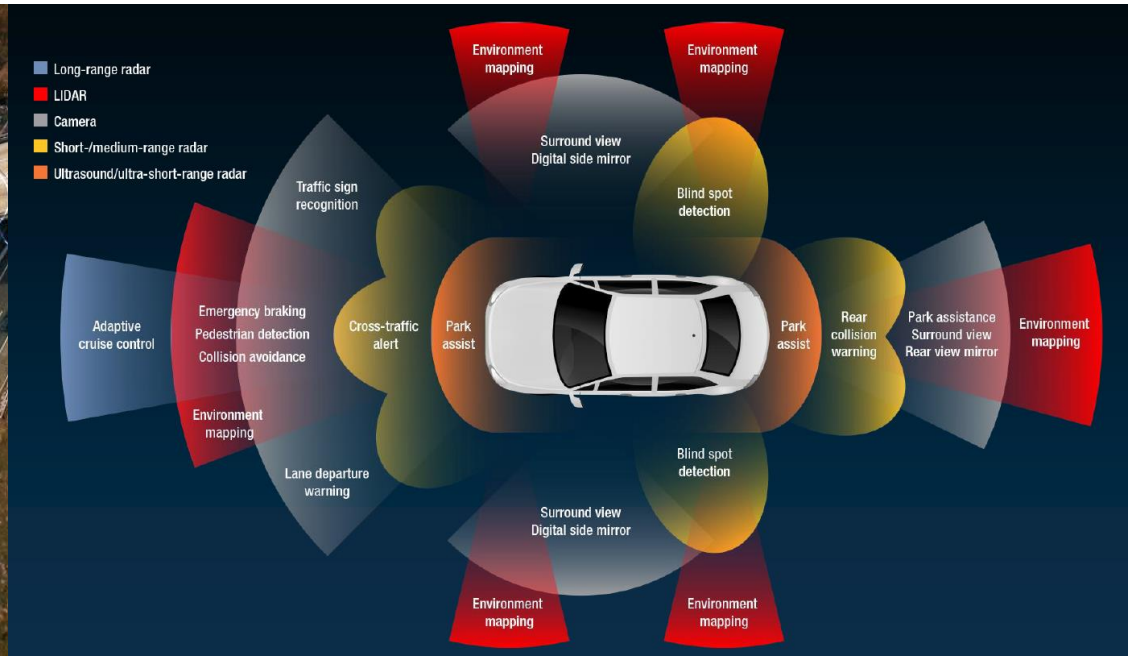


Broad applications

- Entertainment
- Gaming
- Medicine
- Visualization
- Journalism
- Education

Source: Lisa Su, AMD, "Immersive era in consumer computing", IEDM, Dec. 2017

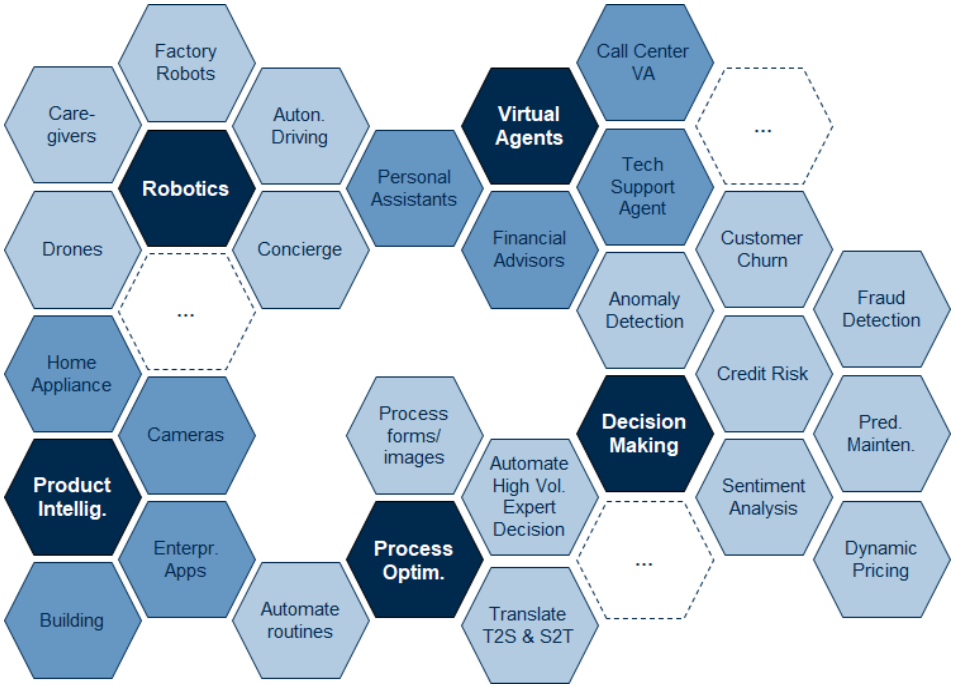
The revolution in automotive



Autonomous and connected cars drive double digit growth to 80 B$ by 2025

Source: NVIDIA Corporate Presentation 2018

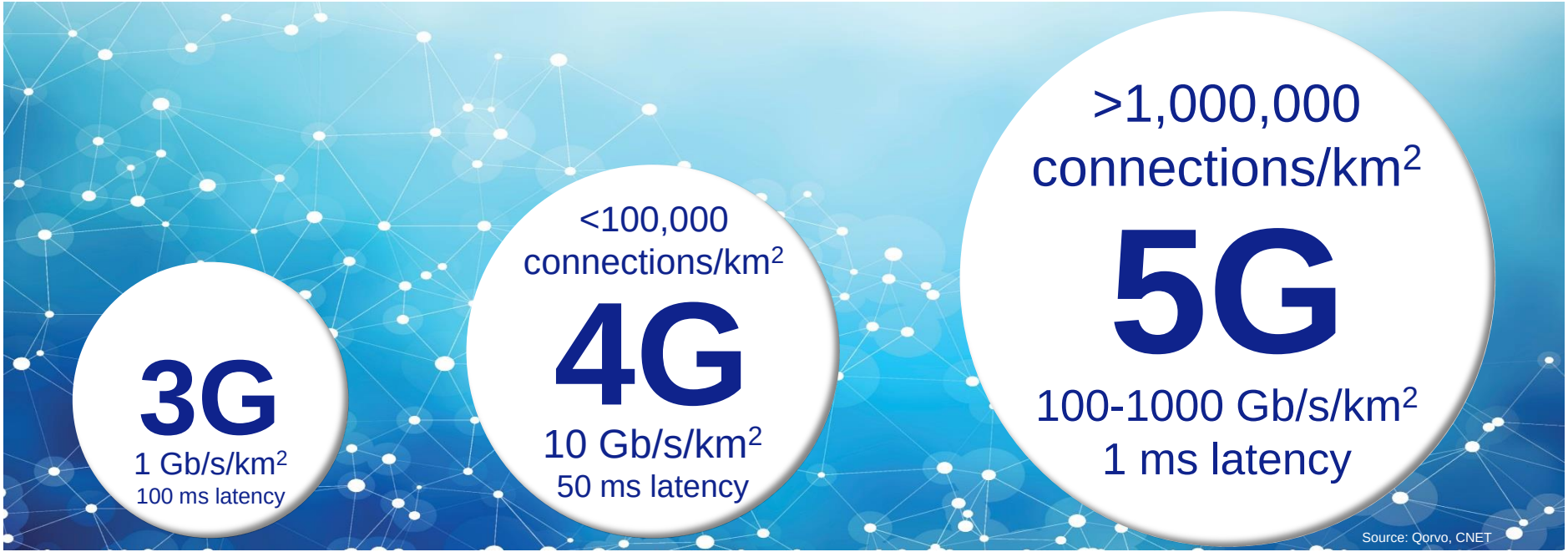
Artificial Intelligence impacting multiple applications



Artificial Intelligence (AI) as a major industry disruptor
will represent a >15B$ new revenue opportunity in semiconductors by 2022

Source: Gartner

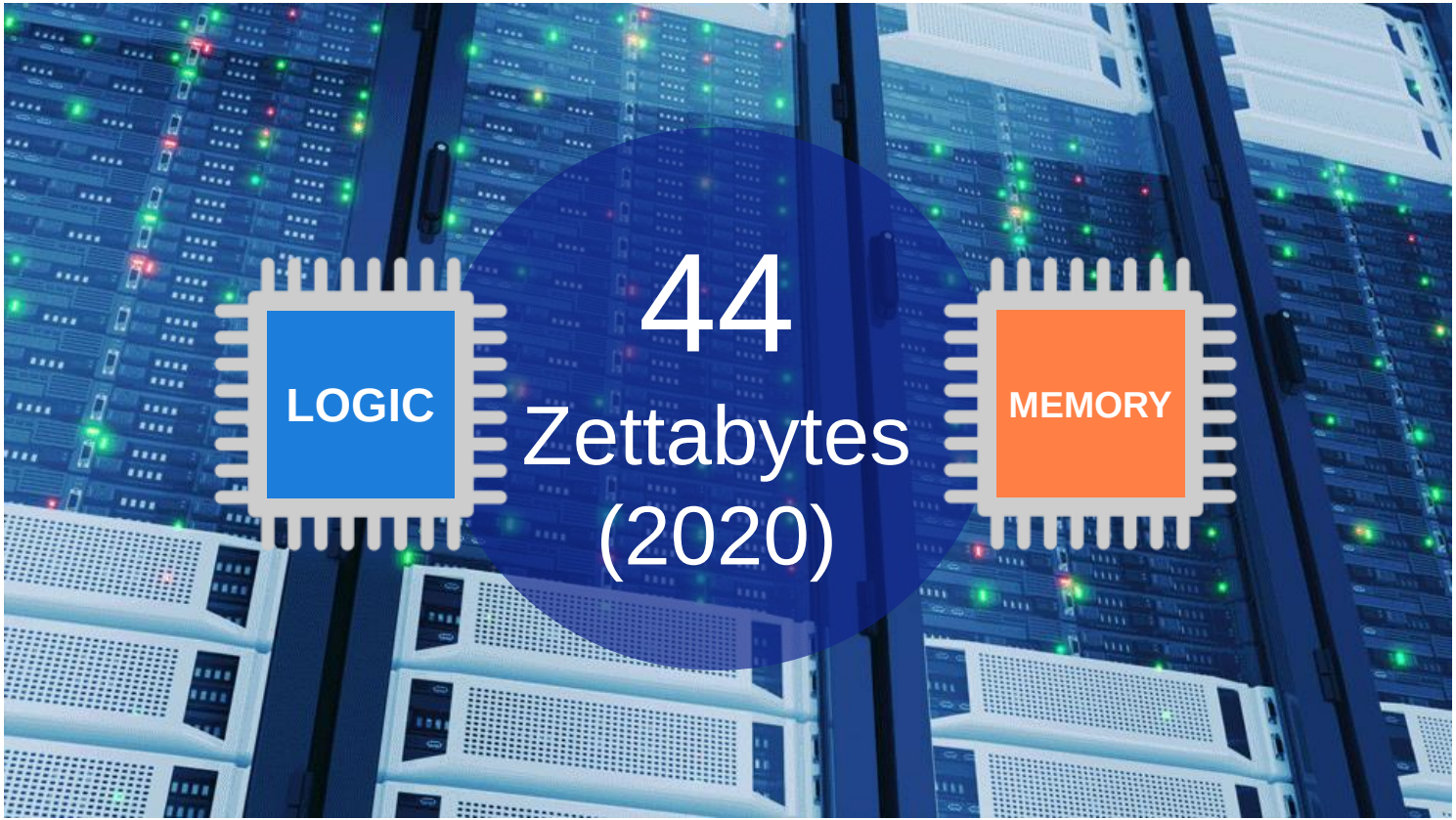
5G connectivity



5G connectivity speed and latency improvement drives applications with more volume and real-time use

Source: Several public sources

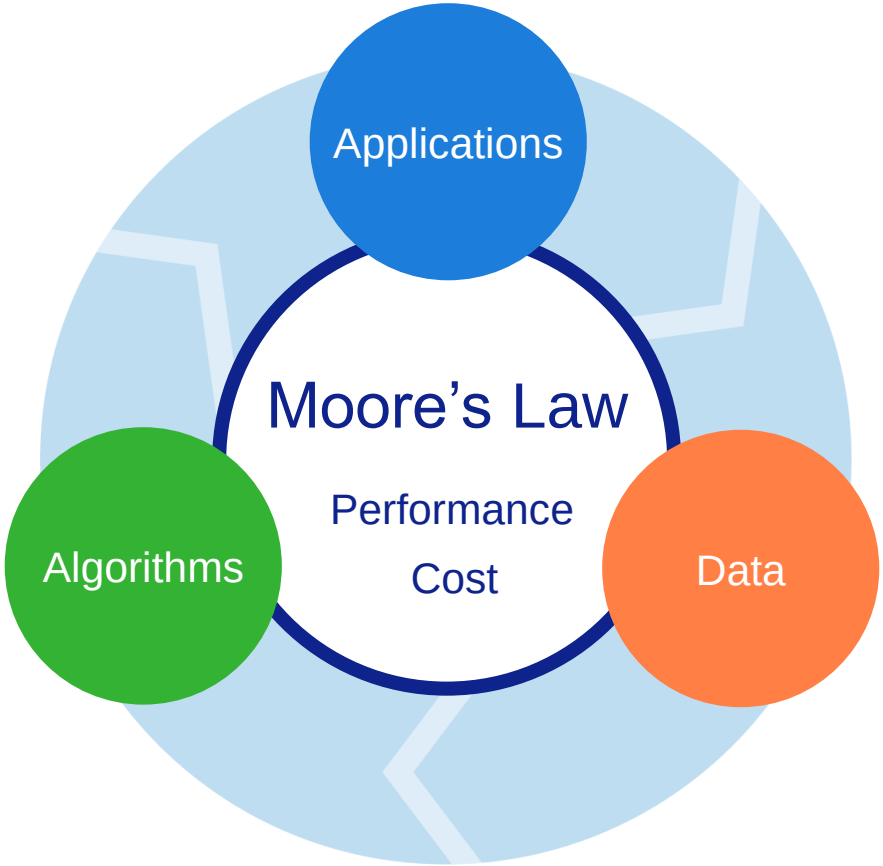
Advanced chips are needed to store and crunch data



1 ZB = 1000^7bytes = 10^{21}bytes = 1000000000000000000000bytes

Source: EMC Digital Universe report with Research & Analysis by IDC (2014)

Major trends in semiconductor-enabled computing



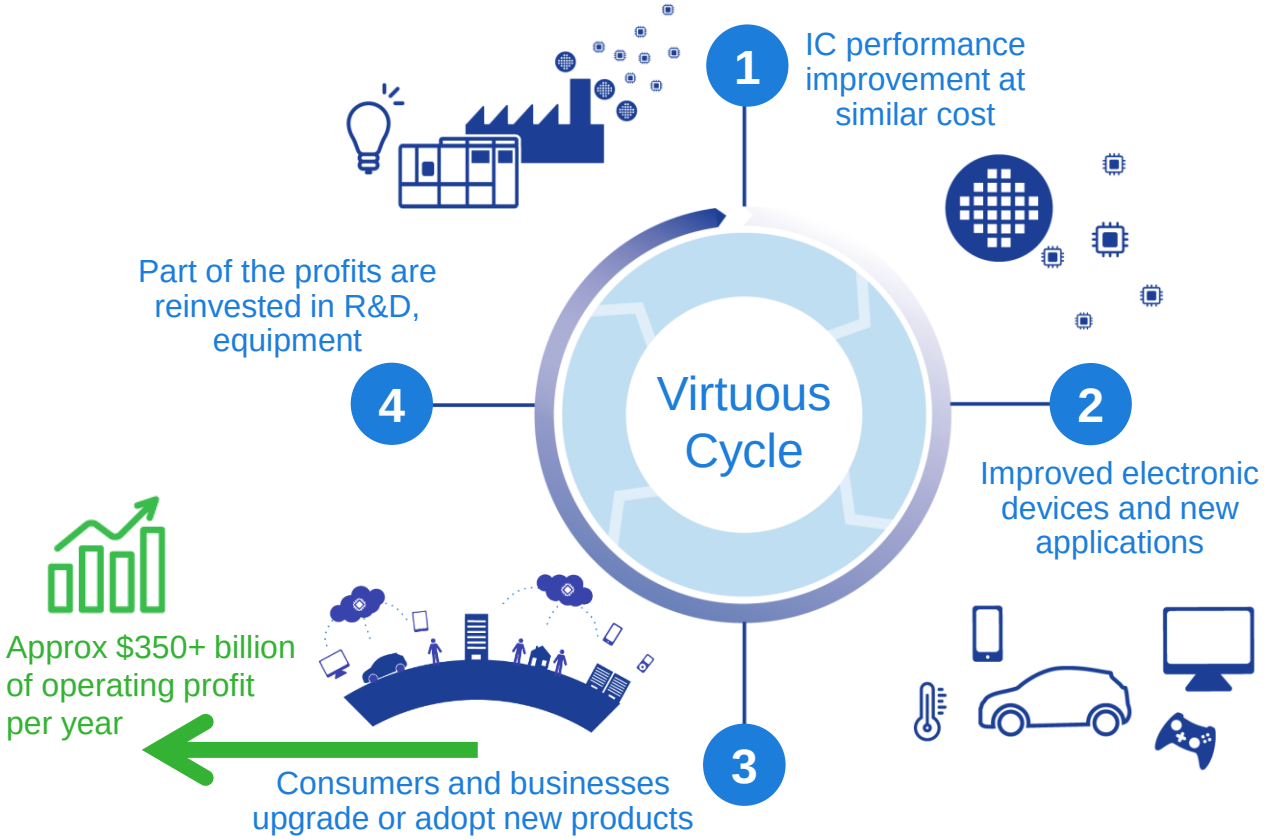
- Autonomous decisions
- Immersive resolution
- On-device Artificial Intelligence
- Virtual / augmented reality

- 5G connectivity
- Real-time latency
- Growing data volumes

- From big data to value
- Enhanced processing
- Deep learning

Considerable motivation to continue Scaling/Shrinking

Moore's Law is underpinning a business model

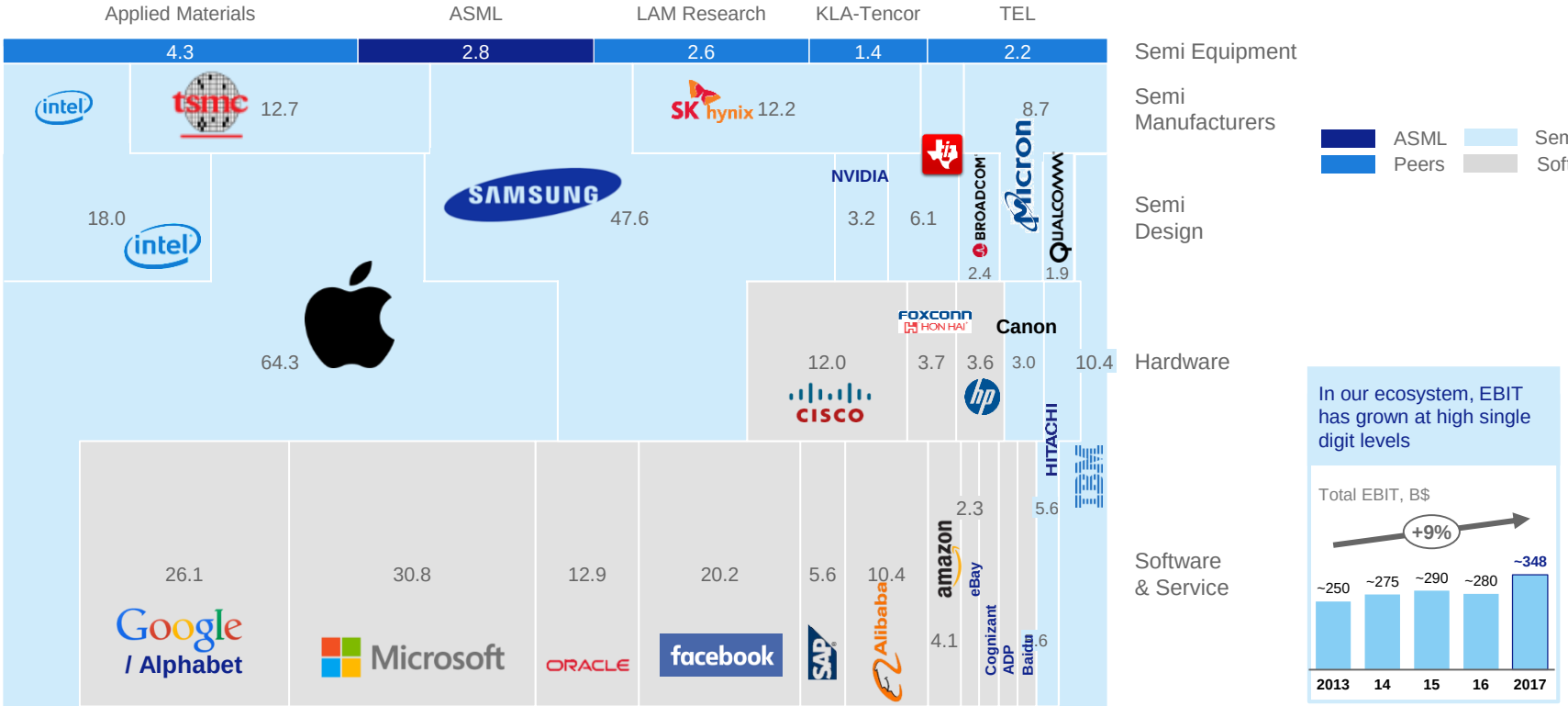


Takeaways

Approx $350 billion of annual profit is riding on the industry's ability to keep this cycle going

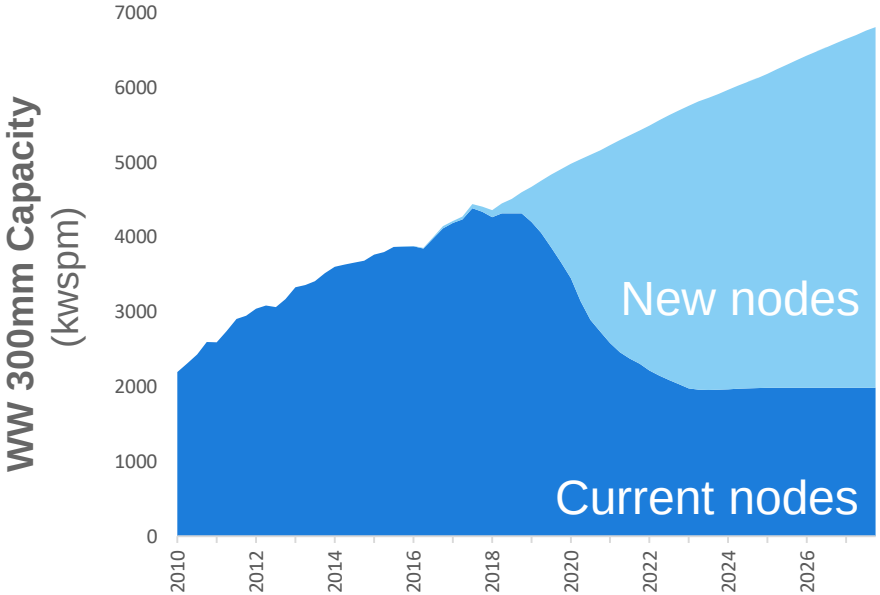
ASML operates in an industry value chain that has considerable means with strong incentives to compete and drive innovation

Top technology companies in our ecosystem (EBIT **CY2017**, B$)

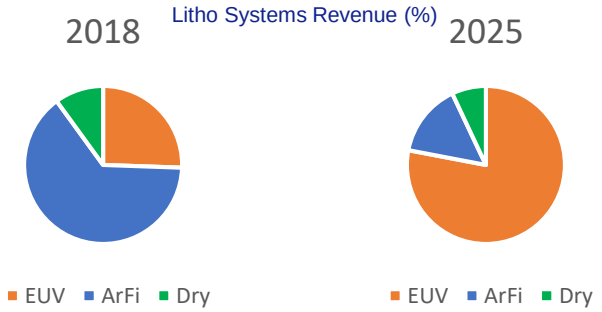


Source: Bloomberg (GICS 45 classification)

New semiconductor nodes drive investments in wafer capacity



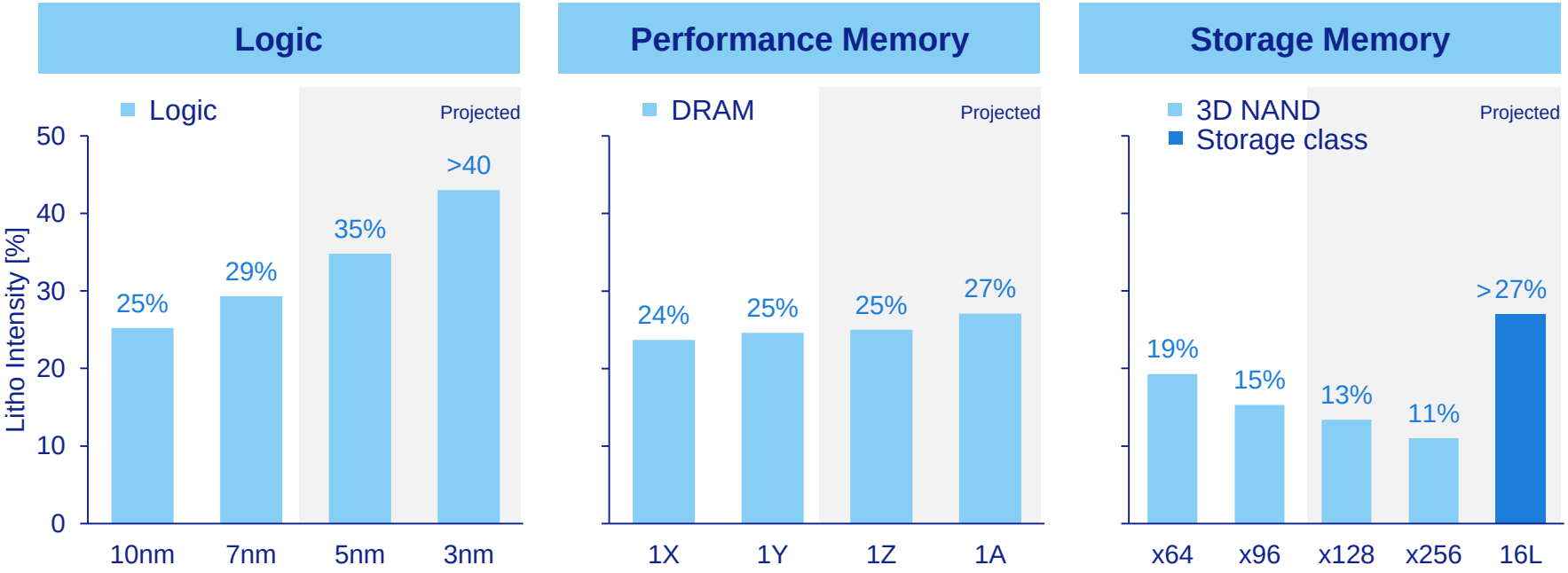
- Growing wafer capacity drives increased litho demand
- New (leading edge) nodes with increased litho intensity further drives litho demand
- Conversion of existing nodes to new nodes also provide additional upgrade opportunity
- New process nodes will be two thirds of the 300mm wafer volume by 2025



Source: ASML analysis

Litho Intensity[1] increasing for Logic and DRAM segments

With 3D XPoint expected to increase intensity for storage memory



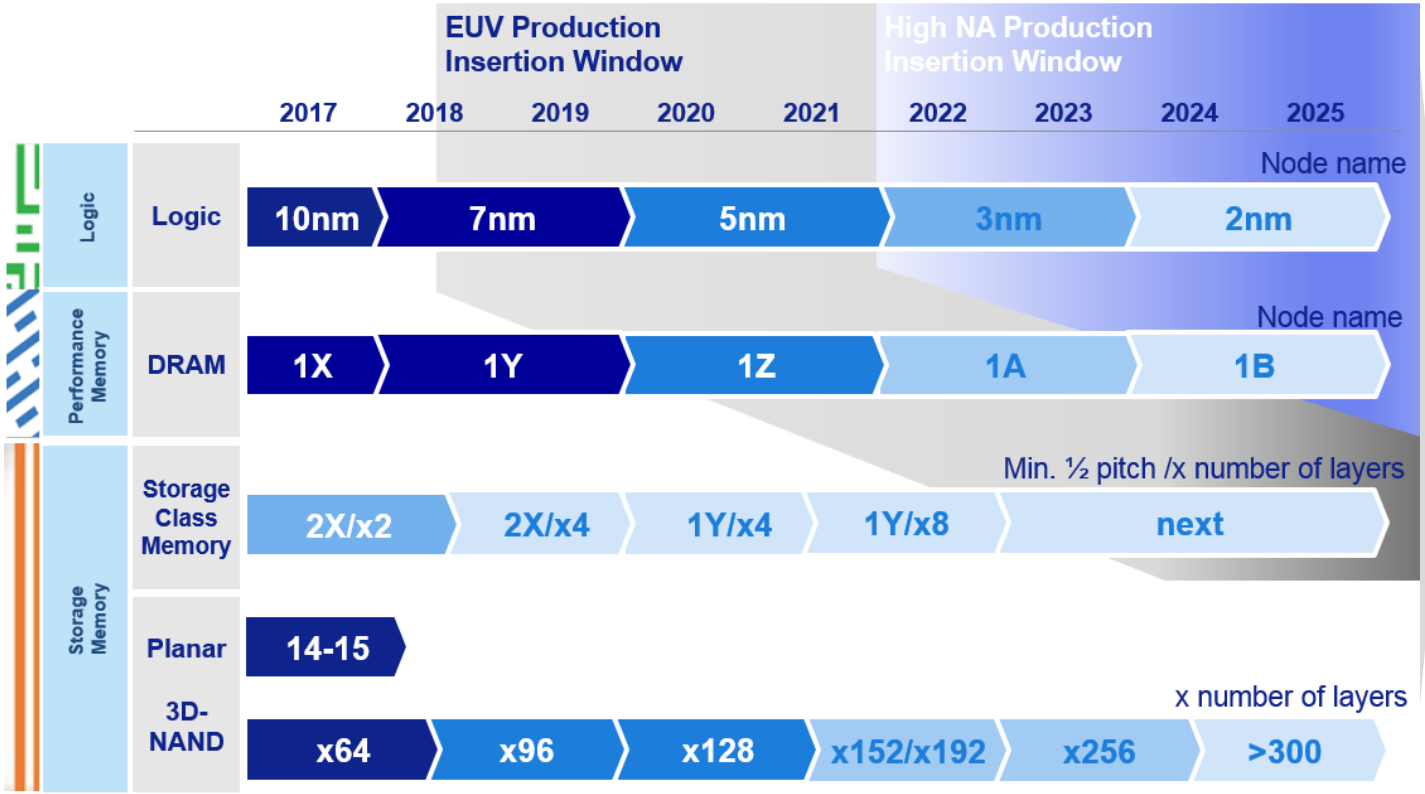
EUV will likely be the enabler of <7nm logic, <1Y DRAM

[1] Litho Intensity = Litho CapEx fraction of total WFE CapEx for Greenfield fab investment

Our strategy addresses opportunity

Opportunity	ASML Strategy	
• Expand our Holistic Litho opportunities	**Holistic Litho extension**	• Strengthen Litho+ leadership with **in device metrology** enabling correction of process induced overlay • Build a winning position in **Pattern Fidelity Control** leveraging e-beam metrology and inspection combined with superior computational Litho and fast stages
• Remain competitive in DUV	**DUV performance**	• Drive **DUV performance** - Continue to lead in innovation - Drive operational cost down and improve up-time - Expand installed base business
• Bring EUV to high volume manufacturing • Extend EUV technology beyond the next decade	**EUV industrialization**	• Deliver on **high volume manufacturing, service and financial** performance • Enhance EUV value for future nodes by **extending NA 0.33 product portfolio down to the 3nm Logic node**
	High NA	• Enable **High NA EUV** at 3nm Logic node, followed by memory nodes at comparable density

To facilitate innovation, technology roadmaps are fully aligned with all key market players



- Industry long-term roadmaps need strategic partnerships to succeed
- ASML key enabler of EUV
- EUV roadmap on track for High Volume Manufacturing in 2018/2019

Today's status

- Production[1]
- Development[1]
- Research[1]
- Roadmap[2]

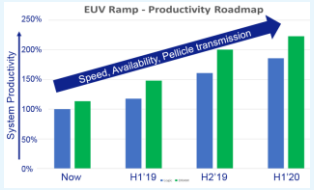
Source: [1] Customers public statements, IC Knowledge LLC; [2] ASML extrapolations

EUV: two accelerated development programs in parallel

after having achieved volume production feasibility metrics

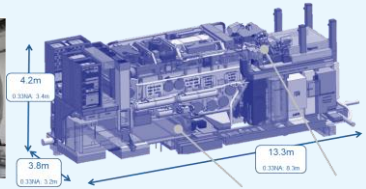
0.33 NA Summary

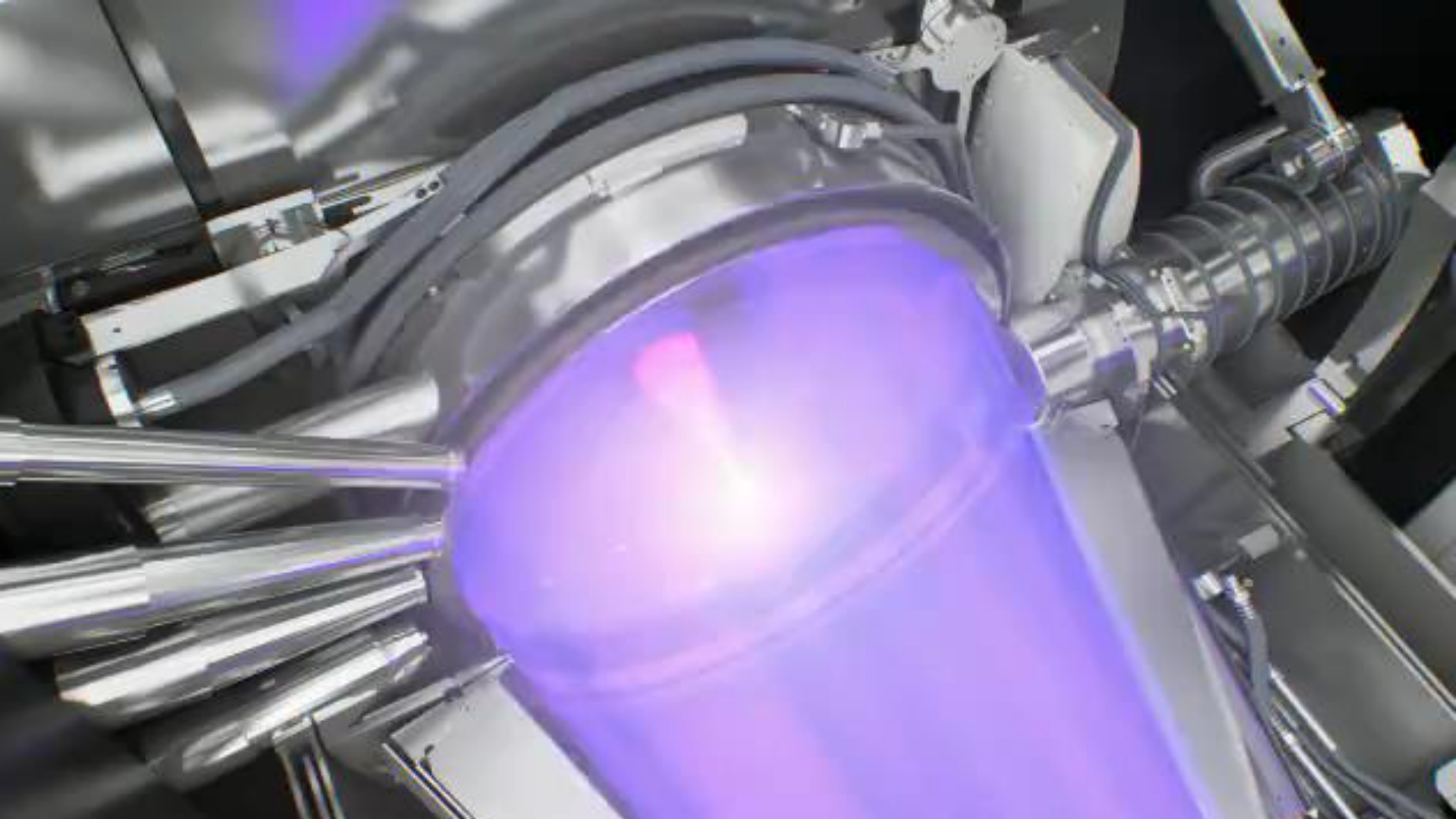
- ASML and supply chain preparing for planned production ramping
- Dedicated focus to improve availability across sites and systems
- Accelerated roadmap of NXE:3400C in order to deliver higher productivity tool, >170wph with improved availability
- Roadmap extended to the 3nm node working mix and match with DUV and High NA using common High NA and 0.33 NA innovations



High NA summary

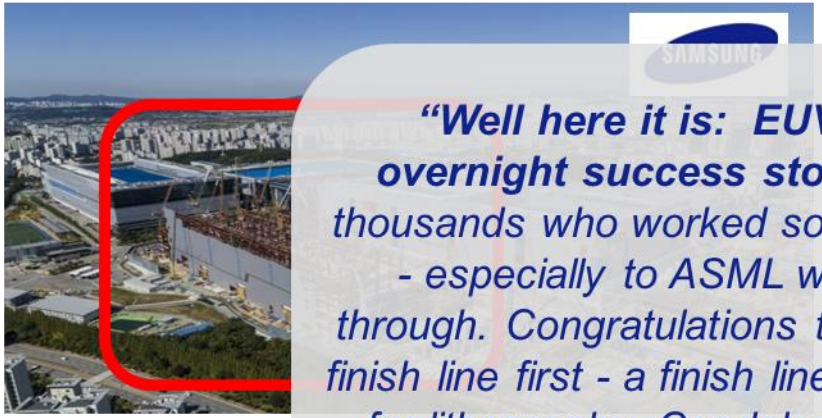
- System design completed, module design progressing and key suppliers selected.
- Customers' roadmap aligned with the High NA introduction plan starting at 3nm.
- Three customers have committed to 4 R&D systems and 8 options for early volume systems. Results in total up to 1.5 B€ Customer commitments
- Design of metrology system by joint ASML-Zeiss team and manufacturing of optics started.
- Extended collaboration with imec in support of necessary developments in ecosystem and demo access for customers





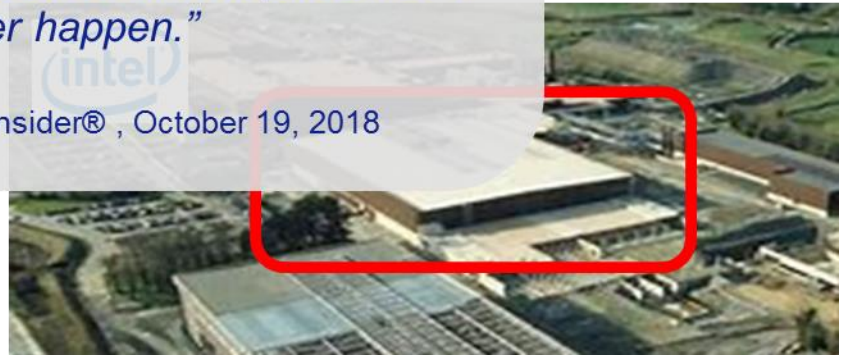
Our customers are not only talking about EUV

Building significant capacity for EUV systems



"Well here it is: EUV is officially a 30-year overnight success story. *Congratulations to the thousands who worked so tirelessly to make it happen - especially to ASML who had the guts to follow through. Congratulations to Samsung for crossing the finish line first - a finish line that starts a whole new era for lithography. Condolences to all who predicted it would never happen."*

Dan Hutcheson, The Chip Insider® , October 19, 2018



TSMC invests 25B$ to move to 5nm, first production early 2020
7nm production has started on track

Renderings of the 2018 iPhones

The chips built using the 7nm process technology are destined for AI, GPU, cryptocurrency, and 5G applications -- totaling 50 chip designs by the end of 2018. For iPhones, the new 7nm process will pave the way for the type of performance improvements customers expect in new iPhones every year.

> *Orders for Apple's custom A12 processor for use in the upcoming iPhones will play a major driver of TSMC's 7nm chip production growth in 2018, according to market sources. The foundry has secured 7nm chip orders from about 20 customers including AMD, Bitmain, Nvidia and Qualcomm. The majority of the orders will be carried out in the first half of 2019, the sources said.*

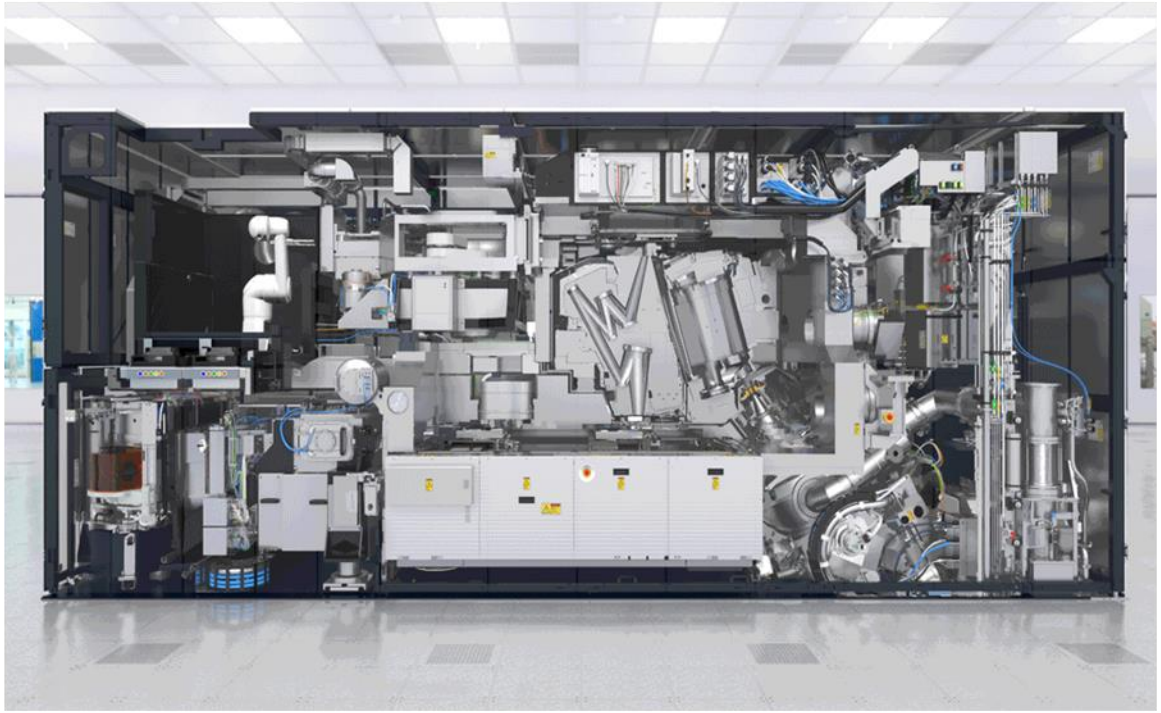
TSMC CEO CC Wei
Photo: Michael Lee, Digitimes, June 2018

At the technology symposium, Wei also said that TSMC is scheduled to move a new 5nm node technology to mass production towards the end of 2019 or early 2020, with plans to invest $25 billion into the technology.

In January, *DigiTimes* reported that Apple selected TSMC to remain the exclusive supplier of the upcoming A12 processor for its 2018 iPhones, following rumors from last summer that Samsung could be returning to iPhone chip production this year. TSMC is the exclusive supplier of the A11 Bionic processor found in the iPhone 8, 8 Plus, and X, as well as the sole supplier of the A10 Fusion processor in the iPhone 7 and 7 Plus.

Source: https://www.macrumors.com/2018/06/22/tsmc-ramps-up-7nm-chips/ https://www.digitimes.com/news/a20180622PD204.html

ASML EUV Lithography value for our customer



Process simplification and improved device performance

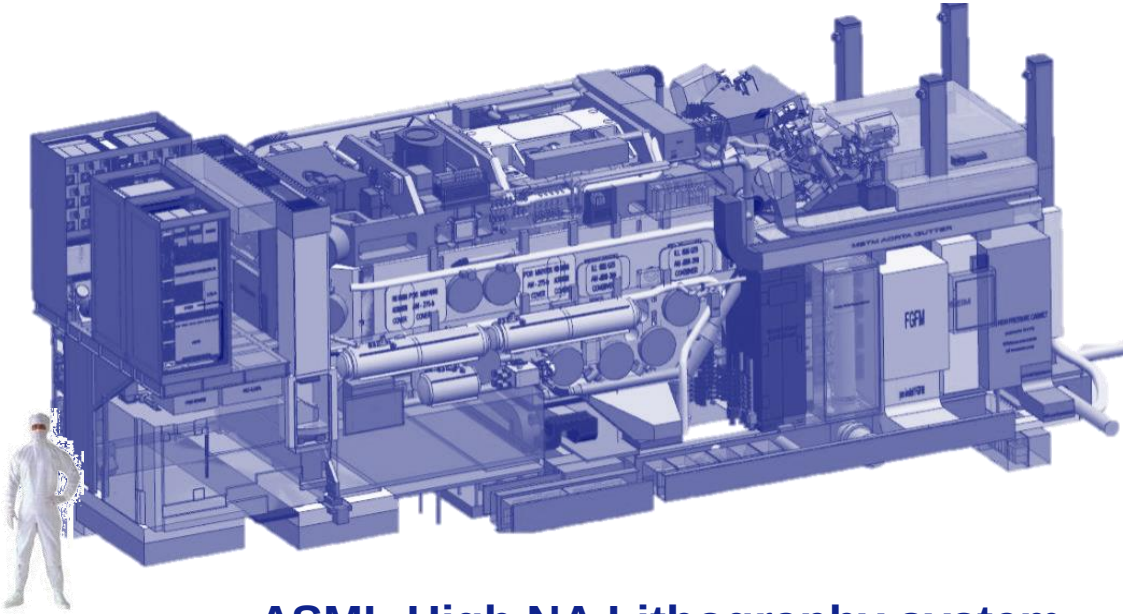
15 to 50% cost reduction compared to multi-patterning schemes

3 to 6x cycle time reduction compared to critical multi-patterning layers

Best in class overlay performance and focus performance

EUV simplifies process complexity to enable our customers to drive cost effective patterning scaling beyond 7nm Logic and 16nm DRAM

In the same way 0.33NA enables 7nm Logic, 0.55NA EUV enables 3nm Logic



ASML High NA Lithography system

Process simplification and improved device performance

>> 50% cost reduction compared to multi-patterning schemes

3 to 6x cycle time reduction compared to multi-patterning for critical layers

Best in class overlay performance and focus performance

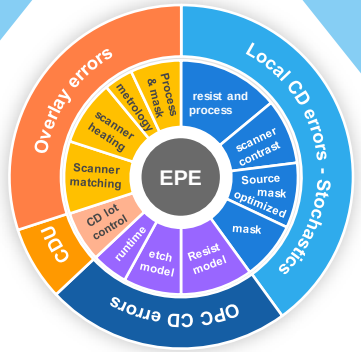
We have received High NA commitment from 3 customers, for a total up to 12 systems

ASML's Holistic Lithography roadmap maximizes patterning performance by optimizing Edge Placement Error (EPE)

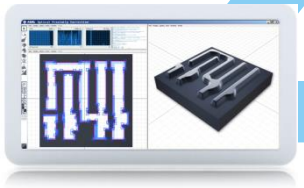
Other patterning tools

Lithography scanner with advanced capability
(imaging, overlay and focus)

Process Window Enhancement



Process Window Control



Computational lithography and metrology

Process Window Detection

Optical and E-beam metrology

Pattern Fidelity Control is next step in holistic lithography

Addition of E-Beam and Etch extends and improves the control paradigm

DUV and EUV Scanner Control

Scanner metrology (100% wafers)

wafers

After-Litho YieldStar Metrology

After-Litho E-beam Metrology

Etch Control

After-Etch YS & E-beam Metrology

Etch Suppliers

Guide to areas of interest

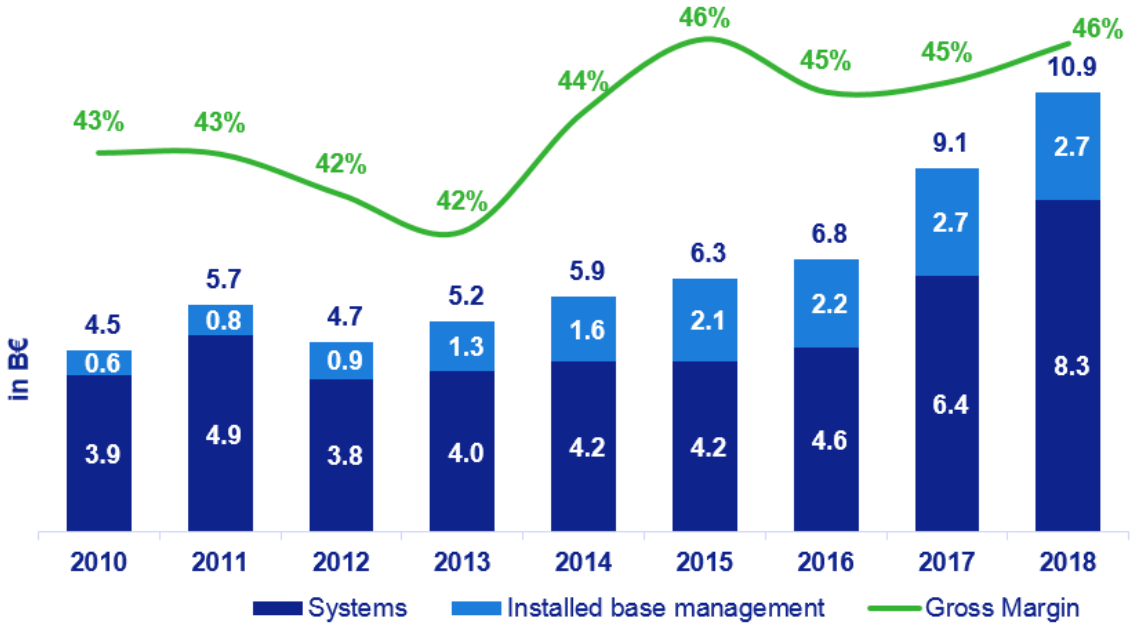
Computational Lithography

Improved algos, models

Scanner
Comp Litho
Optical Metro
E-Beam Metro
Etch

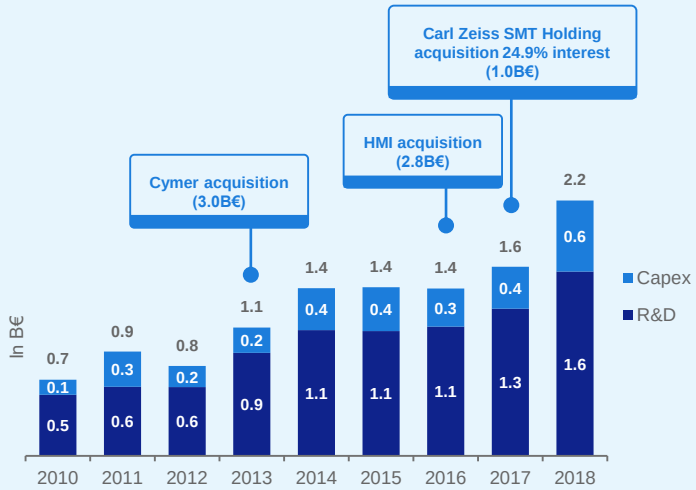
ASML total revenues grew at a CAGR of 12% since 2010

- **Systems revenue** grew at a 10% CAGR since 2010
- **Installed base management**
  - 20% CAGR since 2010 driven by holistic lithography, upgrades and growing installed base
  - Now approximately one quarter of our total revenue
- **Gross Margin trend** reflecting the strength of our DUV and Applications business and progress in EUV profitability

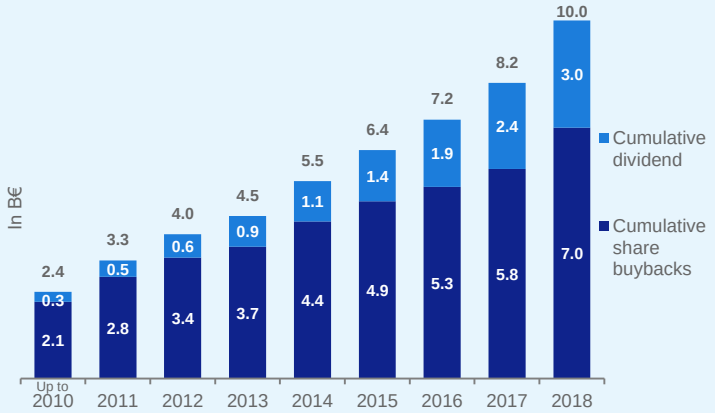


ASML's capital allocation policy

Focused investment in our business through R&D, Capex and strategic M&A



Distribute excess cash to shareholders through a combination of share buybacks and growing dividends



Maintain a strong and flexible balance sheet

ASML updated Financial Model (Investor-day 2018)

	2017 (Actual)	2018 (Guidance)	2020 (CMD 2016)	2020 (Scenario) (Moderate market)	2025 (Scenarios)
Total Sales	9.1B€	~11B€	~11B€	~13B€	~15 - 24B€
Gross margin %	45.0%	~47%	>50%	>50%	>>50%
R&D % sales	14%	~14%	~13%	~14%	~13%
SG&A % sales	5%	~5%	~4%	~4%	~4%
Capex % sales	4%	~6%	~4%	~4%	~3%
Cash Conversion Cycle	224 days	~210 days	<200 days	<200 days	<200 days
Effective Tax Rate	13%	~14%	~14%	~14%	~14%

Executive summary

- Healthy semiconductor **end market growth** driven by **major innovation in semiconductor enabled computing** provides long term growth opportunity
- **Shrink** is a key industry driver supporting innovation and providing long term industry growth
- Holistic Lithography enables **affordable** shrink and therefore delivers compelling value for our customers
- DUV, EUV and Application products are highly differentiated solutions that combined provide **unique value drivers** for our customers and ASML
- **EUV** will **enable** continuation of Moore's Law and will drive long term value for ASML well into the next decade
- ASML models an annual revenue opportunity of **€ 13 billion** in 2020 and between **€ 15 - 24 billion** through 2025
- ASML expects to continue to return **significant amounts of cash** to shareholders through a combination of share buybacks and growing dividends while holding on to its long-held **conservative financial policy**


ASML