Public

EUV Update for UBS Korea Conference 2019

Peter Cheang

Investors Relation, Asia

Seoul, 24 June 2019

Speaker Biography

Peter Cheang

Investment Relations Director, Asia
ASML

Education

- 1995 Santa Clara University, MBA
- 1989 UC, Santa Barbara, MSEE
- 1987 National Taiwan University, BSEE

Work Experience

- 2004 – 2019 Technical Marketing Dir., ASML
- 2000 – 2004 AVP, Director, Win Semiconductor Corp.
- 1998 – 2000 Sr. Mktg.. Mgr., ASML
- 1994 – 1998 Prod. Mgr., Ultratech Stepper Inc.
- 1989 – 1994 MTS, Samsung Microwave Semiconductor US

EUV development has progressed over >30 years

from Research to HVM insertion

HVM = High Volume Manufacturing

EUV consortia

1st lithography (LLNL, Bell Labs, Japan)

ASML starts EUVL research program

ASML ships 2 alpha demo tools: IMEC (Belgium) and CNSE (USA)

ASML ships 1st pre-production system NXE:3100 (NA 0.25)

ASML ships 1st system NXE:3300B (NA 0.33)

ASML ships 1st HVM system NXE:3400B (NA 0.33)

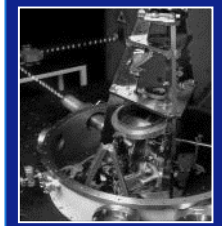
EUV-LLC (USA)

'85 '86 '87 '88 '89 '90 '91 '92 '93 '94 '95 '96 '97 '98 '99 '00 '01 '02 '03 '04 '05 '06 '07 '08 '09 '10 '11 '12 '13 '14 '15 '16 '17 '18

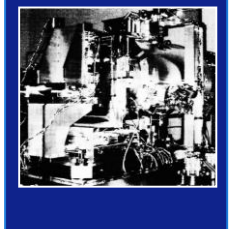
Euclides

MEDEA (EU)

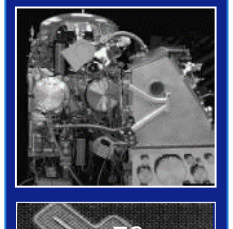
NL



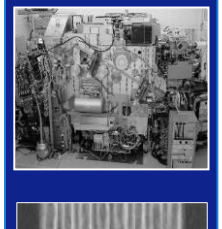
Japan



USA



NL



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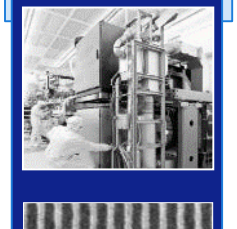

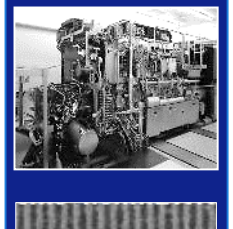

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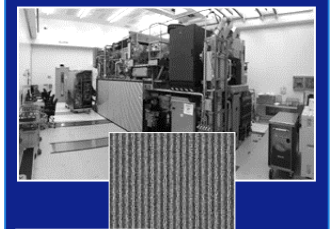


ASML EUV Lithography product and business opportunity

Key Messages

ASML EUV lithography extends our Logic and DRAM customers roadmap by providing lithography resolution improvement, state of the art overlay performance and year on year cost reduction

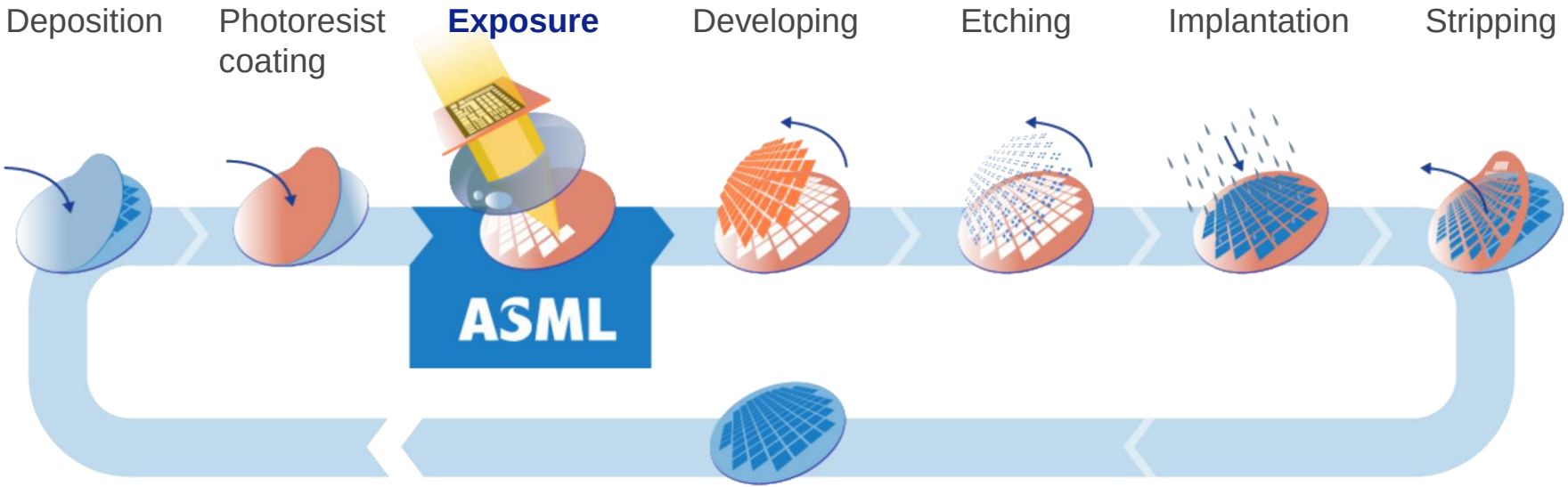
Our customers are preparing for EUV ramp at 7nm Logic node and 16nm DRAM node with systems deliveries and qualification on-going. EUV layers adoption continues to grow to reduce patterning complexity and cost

EUV industrialization is well underway to meet our customers requirements for availability, productivity, yield in high volume manufacturing. The necessary eco-system is also in place to support our customer EUV Ramp

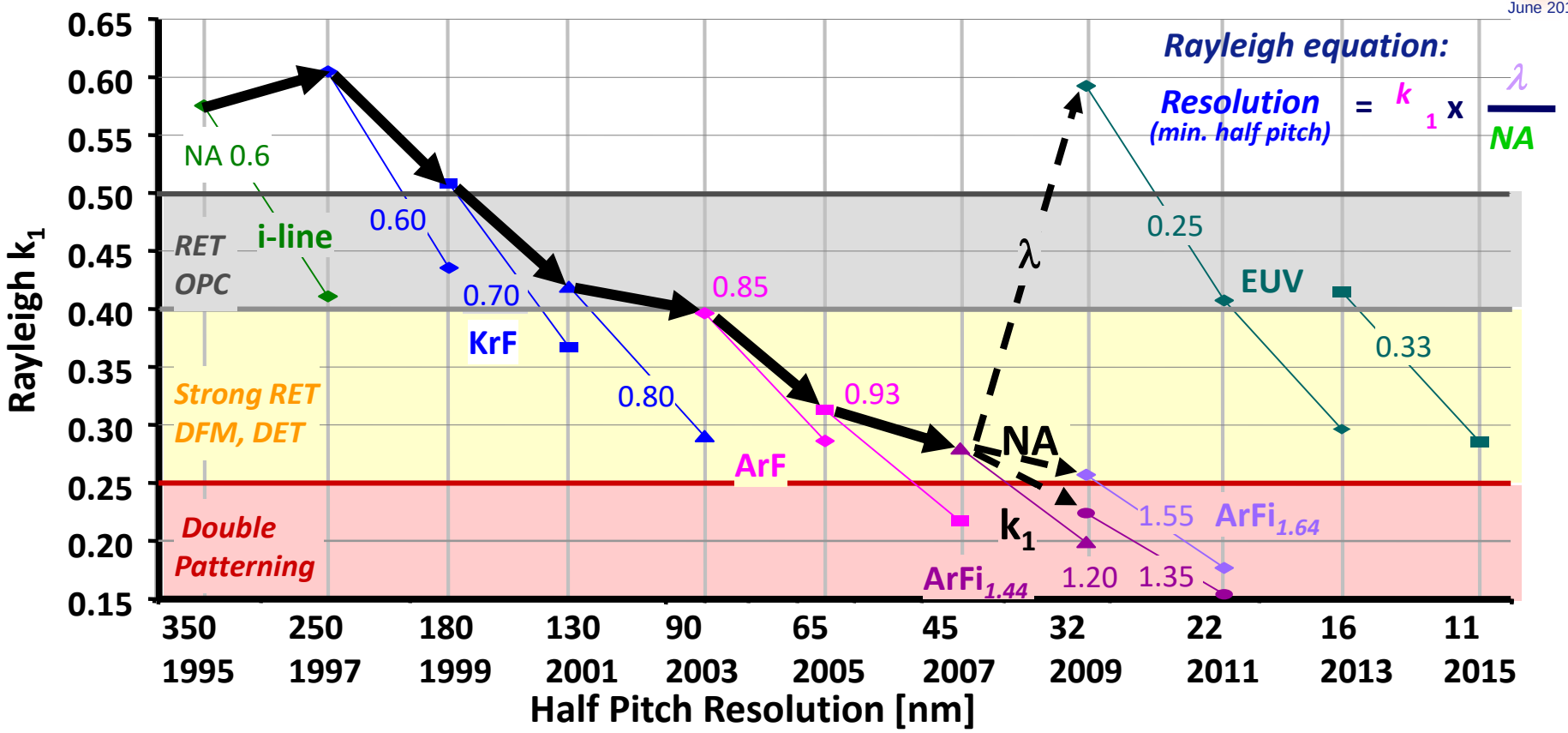
EUV product roadmap will extend our 0.33NA EUV platform and introduce 0.55NA EUV platform in parallel to provide comprehensive and flexible solutions to our customers' continuous demand for patterning scaling well into the next decade

Lithography Process

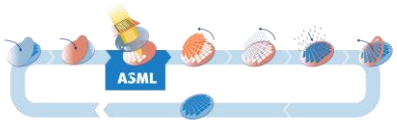
The chip manufacturing loop relies on ASML



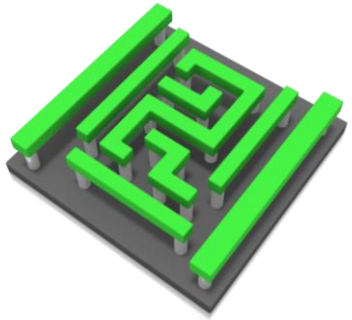
Key performance enablers for lithography shrinkage



EUV provides patterning simplification compared to multi-patterning immersion



EUV



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Single exposure

Process Steps
- CMP
- Dry Etch
- Metrology
- Lithography
- Track
- Deposition
- Clean
- Hard mask

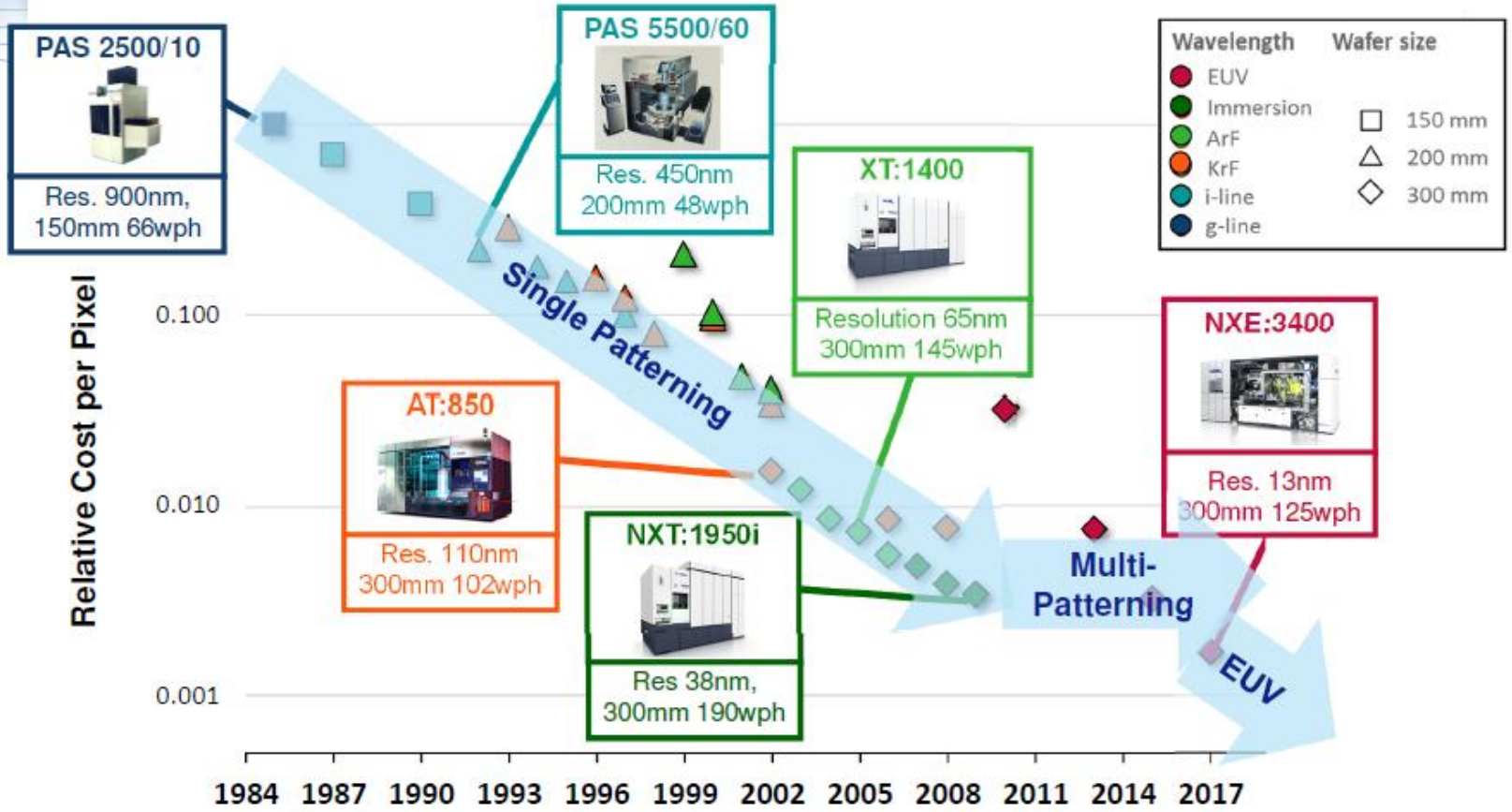
LE3 = 3x Litho-Etch, “Triple patterning”

LE4 = 4x Litho-Etch, “Quad patterning”

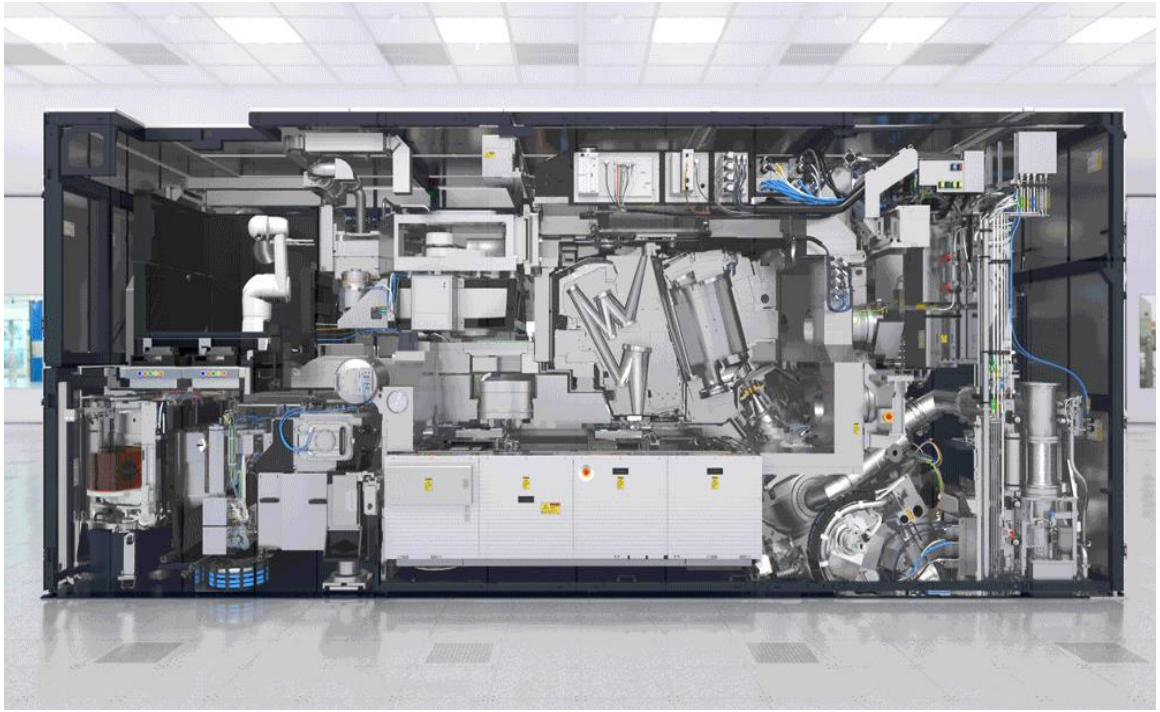
SAQP = Spacer Assisted Quad Patterning

Cut = Separate Litho-Etch step

EUV enables continued Litho cost reduction



ASML EUV Lithography value for our customer



Process simplification and improved device performance

15 to 50% cost reduction compared to multi-patterning schemes

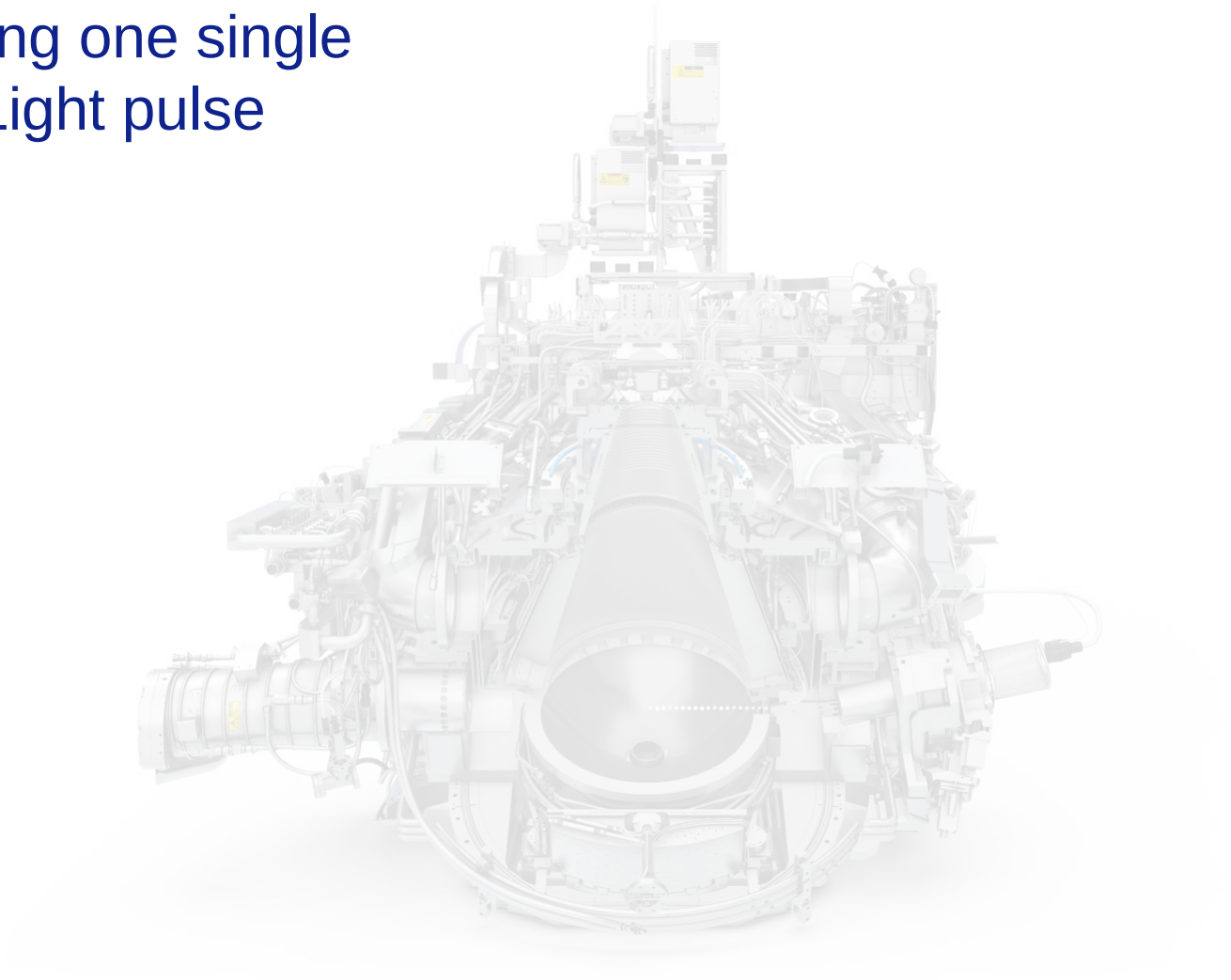
3 to 6x cycle time reduction compared to critical multi-patterning layers

Best in class overlay performance and focus performance

EUV simplifies process complexity to enable our customers to drive cost effective patterning scaling beyond 7nm Logic and 16nm DRAM

How EUV photon is generated

Creating one single EUV Light pulse



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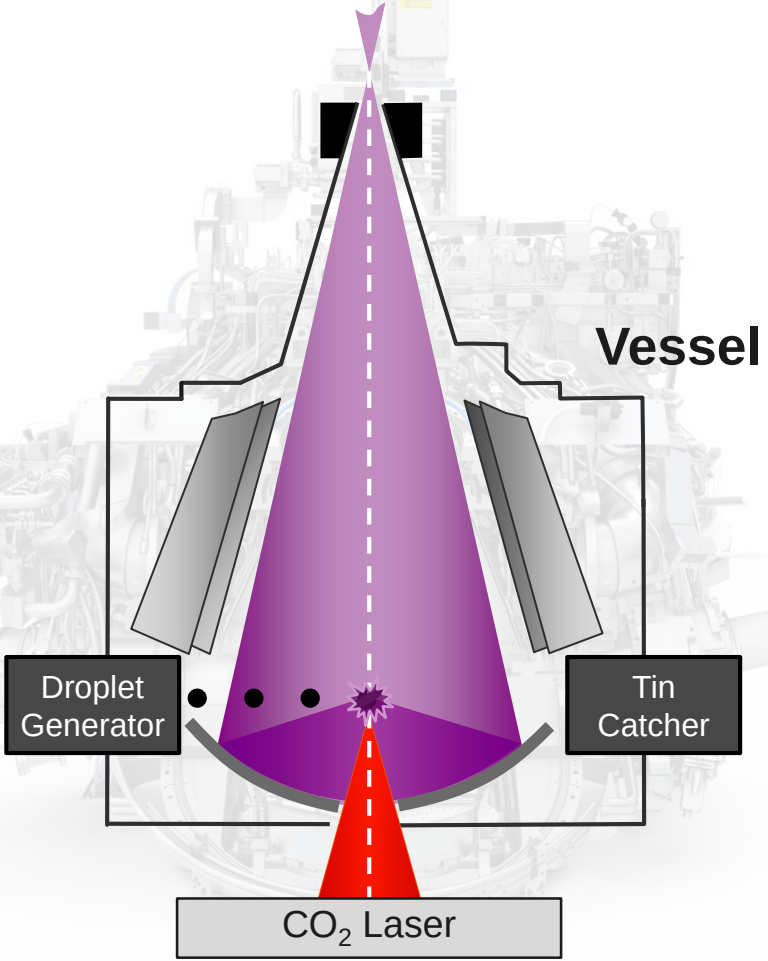
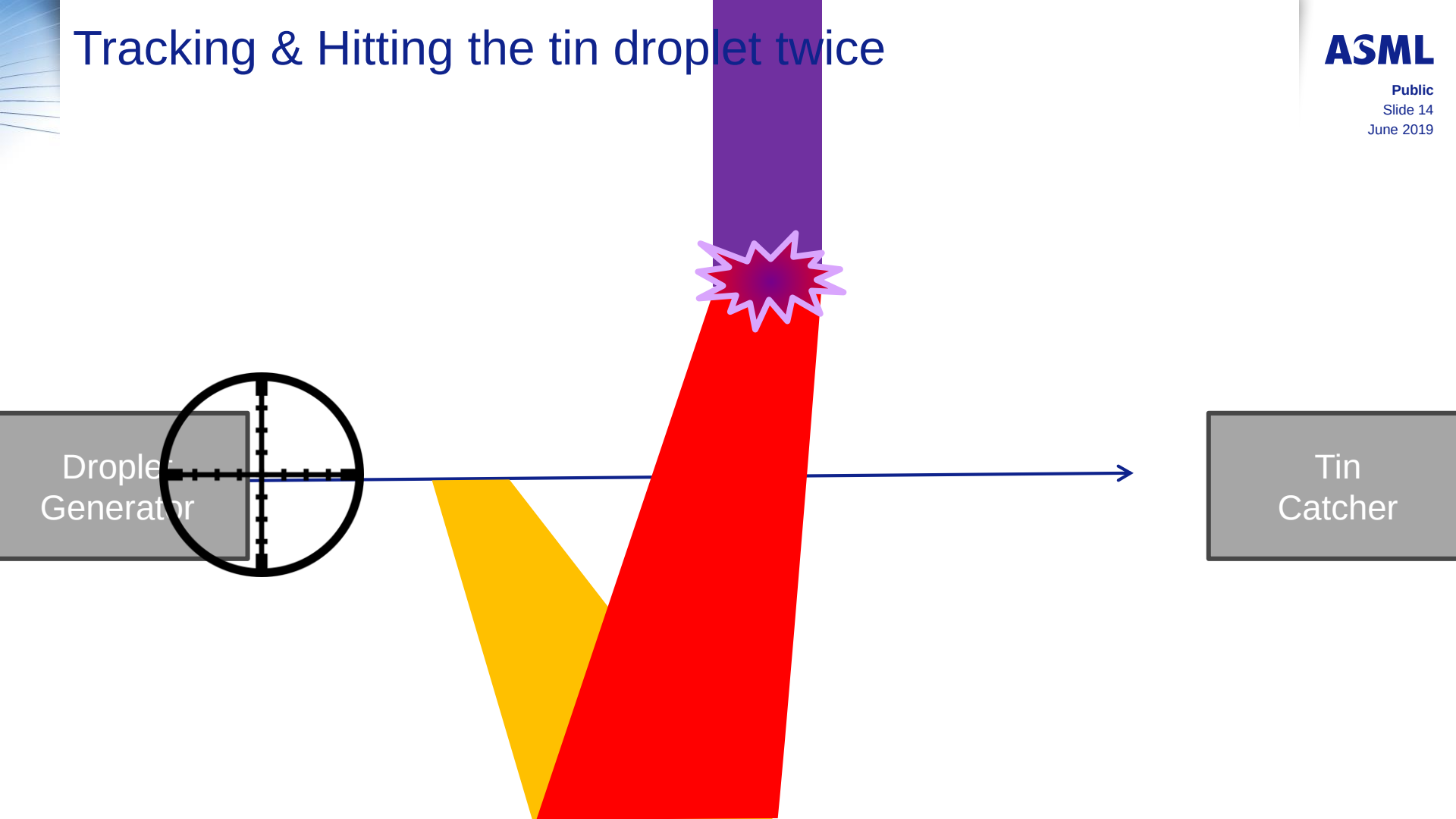
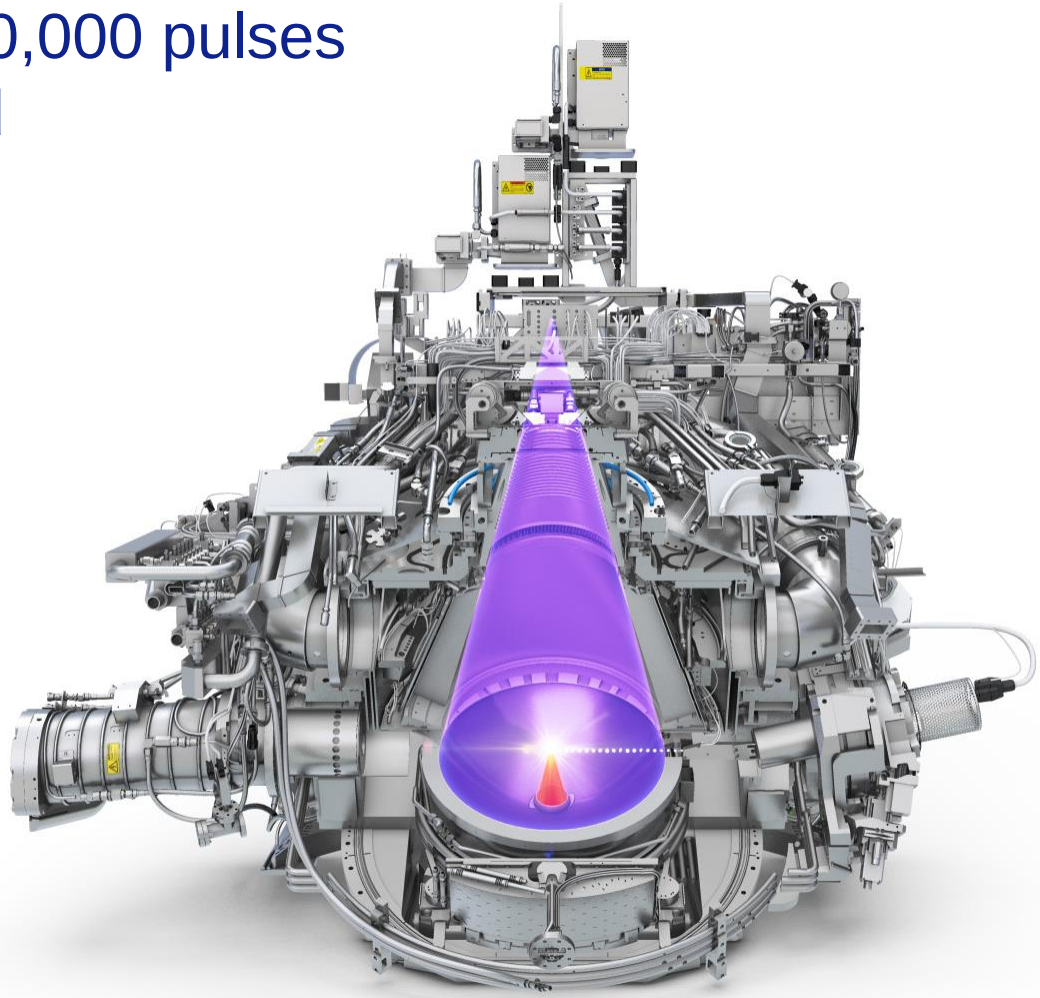


Tracking & Hitting the tin droplet twice

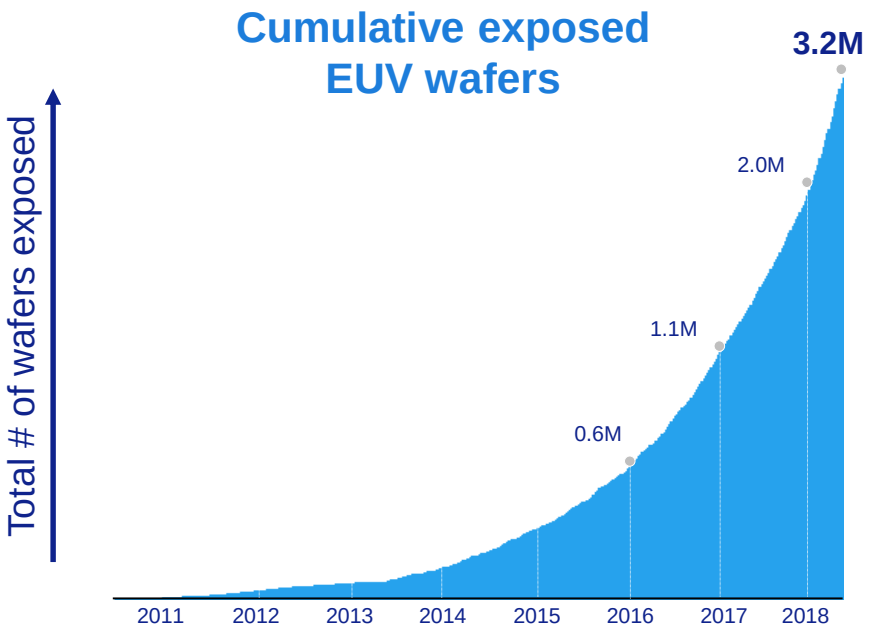


Creating 50,000 pulses per second



EUV for HVM: Status and Opportunities

EUV ramp at our Logic customers has started with production in Logic and DRAM expected in 2019



C.C.Wei, TSMC co-CEO @ 2Q18 earnings (July 2018)

"The silicon results from our N7+ today are very encouraging. Volume production will start Q2 next year, that is Q2 2019. We have made ready multiple EUV scanners to support not only the N7+ development, but also N5 development. Our silicon data have proved all the benefits we expect from process simplification with EUV. In addition, we have also started our N3 technology development."

ES Jung, EVP Foundry
Seoul October 18th, 2018

The initial EUV production has started in Samsung's S3 Fab in Hwaseong, Korea. By 2020, Samsung expects to secure additional capacity with a new EUV line for customers who need high-volume manufacturing for next-generation chip designs

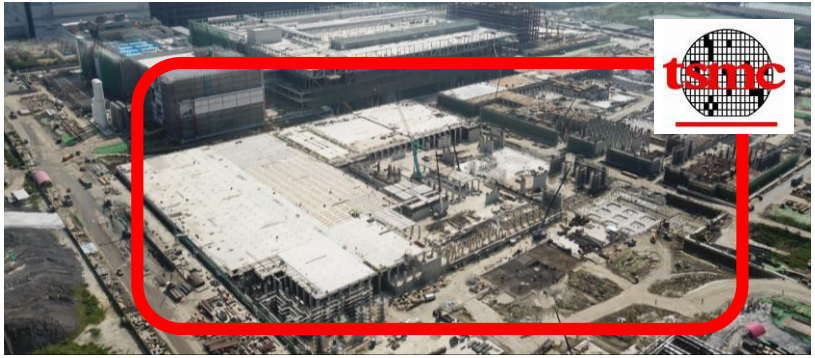
Intel @ 1Q18 earnings (April 2018)

"…10 nm process…volume production is moving from the second half 2018 into 2019... we understand the yield issues. They're really tied to this being the last technology not having EUV, the amount of multi-patterning and the effect of that on defects…we have 4,5,6 layers of patterning to produce a feature.

More than 3.2 Million wafers run since 2011…
… ~1 Million in the last 6 months

Our customers are not only talking about EUV

Building significant capacity for EUV systems



EUV estimated demand per fab by market

Range of layers and corresponding systems per fab[1]

Market	Fab Capacity (kwspm[2])	EUV layers	EUV systems/fab
Logic (7nm – 5nm)	45	10 – 20	10 – 20
DRAM (16nm -1Anm)	100	1 - 6	2 - 10

Logic EUV capacity:

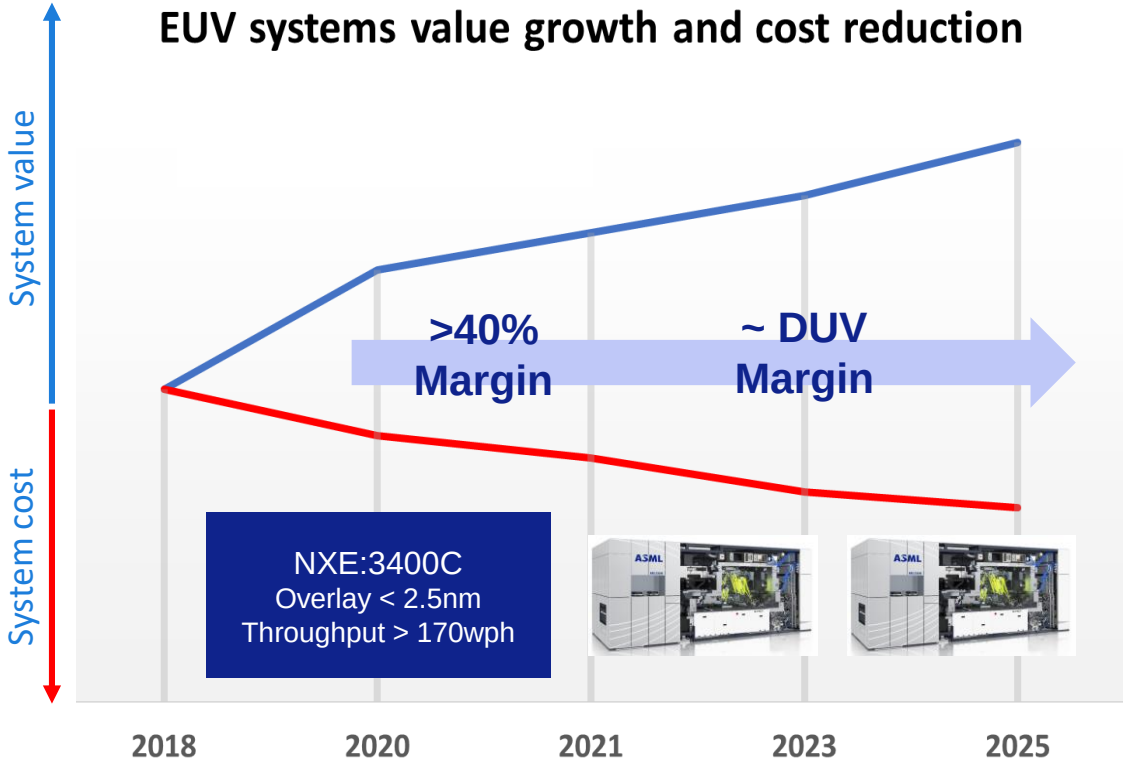
1 EUV layer requires 1 EUV system for every 45k wafer starts per month

DRAM EUV capacity:

1 EUV layer requires 1.5 to 2 EUV systems for every 100k wafer starts per month

[1] "Typical" process and system conditions in the 2018-2022 timeframe, not specific customer condition
[2] kwspm: x1000 wafer starts per month

Expect EUV value increase and cost reduction to bring EUV gross margin to comparable level as DUV



Increased Customer Value

- Productivity improvement (availability & wafer per day)
- Overlay and Imaging improvement
- Process simplification & improved device performance
- Node to node system upgrades

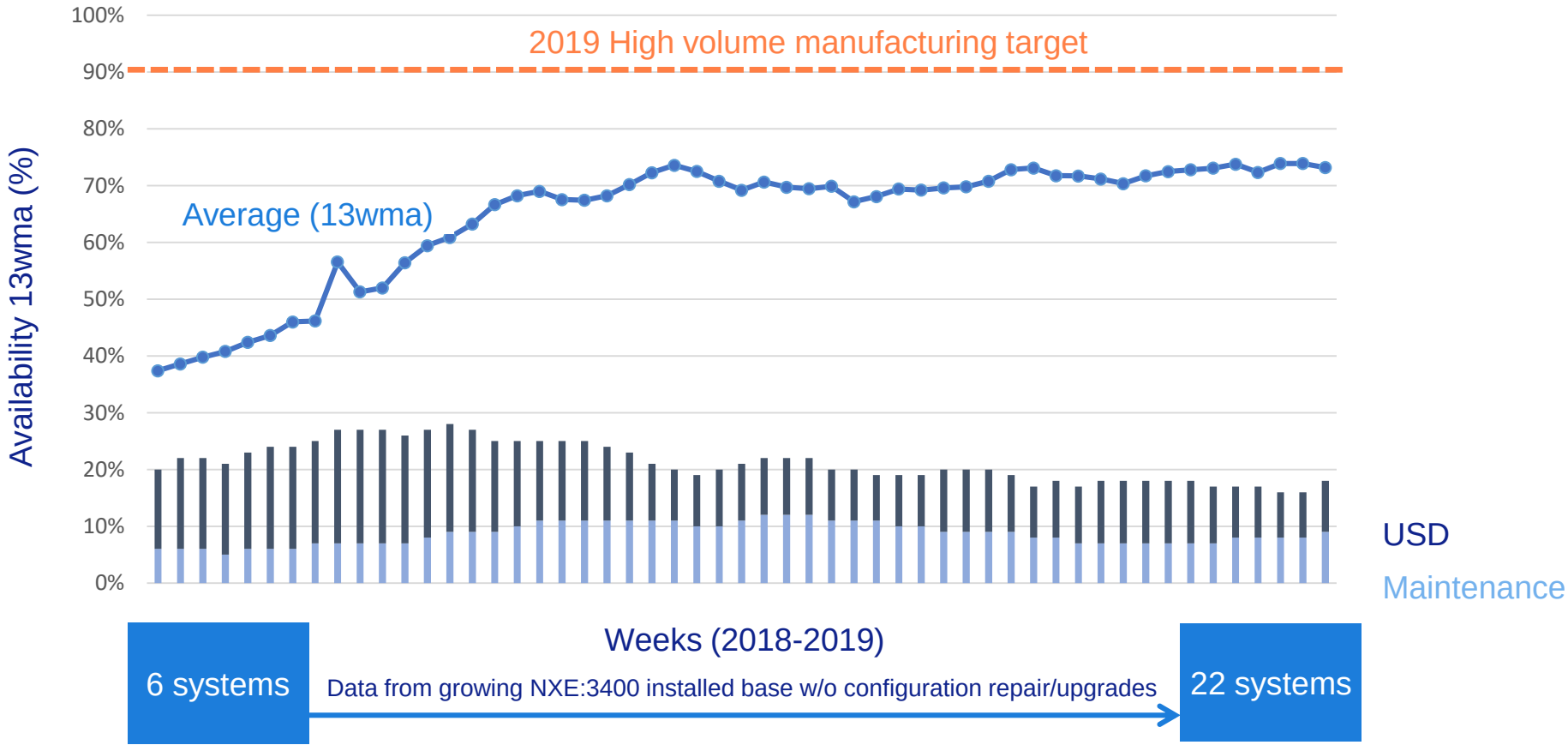
Reduced system cost

- Higher utilization of existing infrastructure
- Cycle time reduction
- Material cost reduction

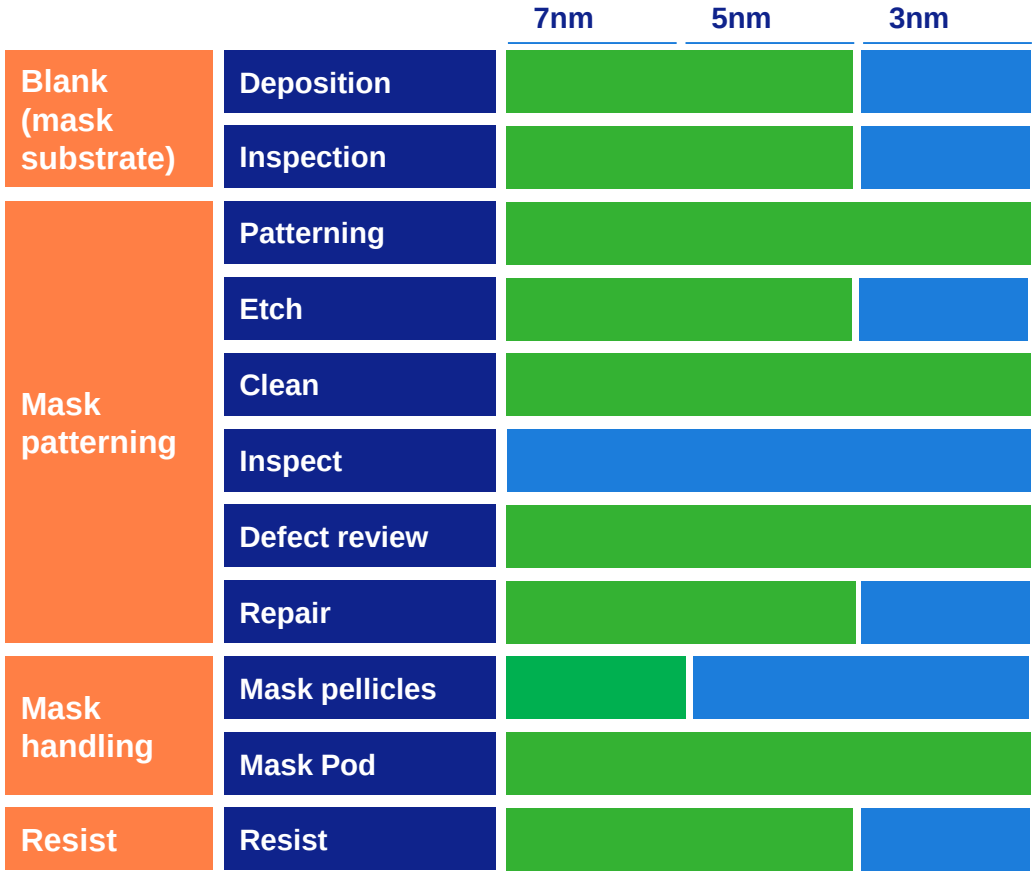
HVM Readiness

NXE:3400B's availability substantially improved

Growing installed base further improvements planned



EUV infrastructure viable for 7nm and 5nm Logic nodes and DRAM, improvements on-track for 3nm



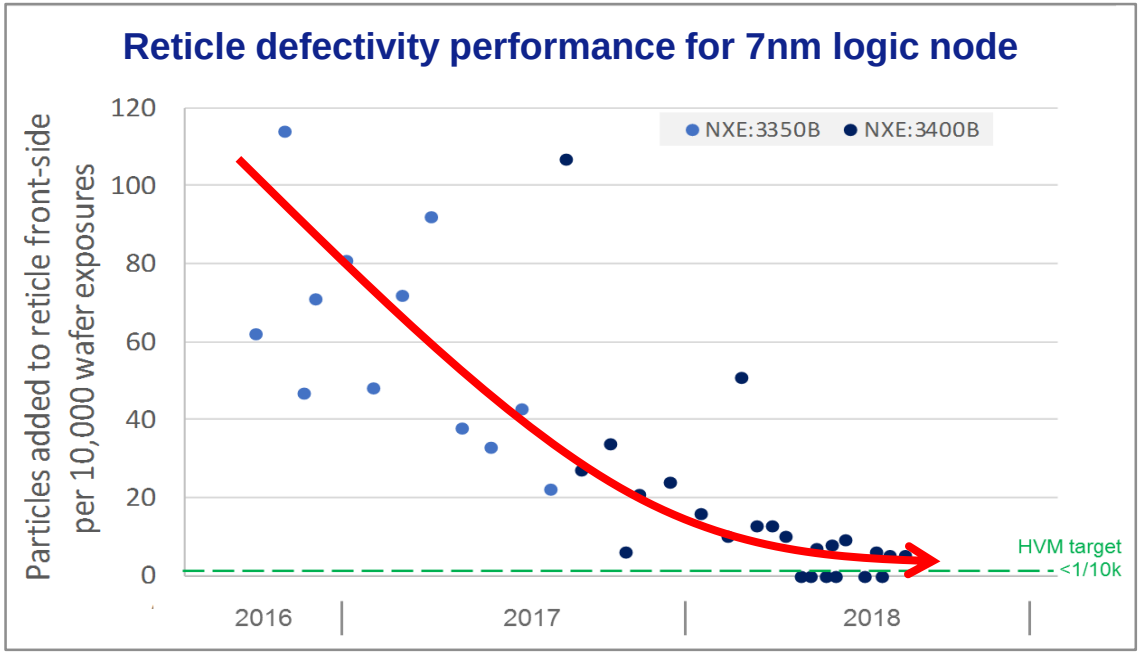
Players include

Veeco, Applied Materials, KLA-Tencor, Lasertec, NuFlare, JEOL, IMS, Applied Materials, SUSS MicroTec, Applied Materials, KLA-Tencor, HMI, NuFlare, Lasertec, Lasertec, Zeiss, Zeiss, RAVE, Hitachi Inspire the Next, ASML, Entegris, 家登精密, JSR, Shin-Etsu, tok, Inpria

Secured
Improvements req'd

EUV scanner defectivity performance and pellicles support manufacturing requirements

DRAM, Logic non critical EUV layers: no Pellicle



EUV Defectivity level <5 adders / 10,000 wafers exposures, support HVM requirement for Non critical EUV layers

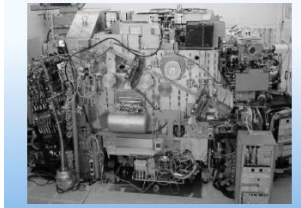
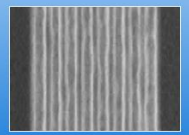
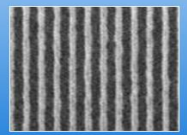
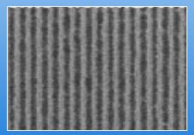
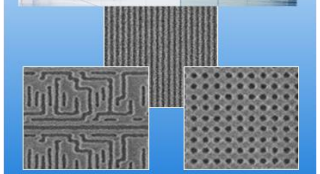
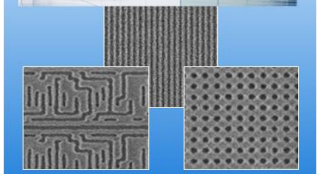
Critical layers: pellicle

	2018	2019
Transmission		
Life time (wafer)		
CD performance		

Secured
Improvements req'd

EUV Roadmap

Our EUV journey so far…. > 10 years to develop EUV technology with our customers

2006	2010	2013	2017	2018-19
ASML ships first full field EUV research system	ASML ships first NA 0.25 development system NXE:3100	ASML ships first NA 0.33 development system NXE:3300B	ASML ships first NA 0.33 production system NXE:3400B	ASML NXE:3400B installed base >25 systems by end of 2018
				
				
28 nm Lines and spaces	19 nm Lines and spaces	13 nm Lines and spaces	7 nm and 5 nm node patterns	7 nm and 5 nm node patterns

Number of tools	2	8	10	>25
Availability	<10%	40%	70%	80% → 90%
Productivity	<1wph	<10wph	<50wph	125 → 155wph
Overlay	8nm	6nm	5nm	3nm →2.5nm

EUV technology extended for both 0.33NA and 0.55NA

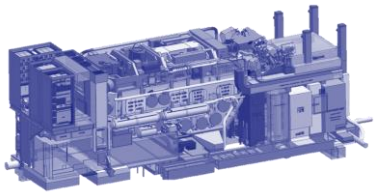
Supporting applications beyond the next decade

EUV 0.33 NA

EUV 0.33 platform will be extended to provide state of the art overlay and node to node productivity improvements

	2016	2017	2018	2019	2020	2021	2022	2023	…2025
EUV 0.33 NA 13nm	**NXE:3350B** 2.5 | 125wph	**NXE:3400B** 2.0nm | 125wph	**Overlay** 1.5nm	**TPut[1]** 155	**NXE:3400C** 1.5nm | 170wph		**NXE Next** <1.7nm | ≥ 185wph		
0.55 NA 8nm									**High NA** 1.7nm | 185wph

Product
Matched Machine Overlay|Throughput

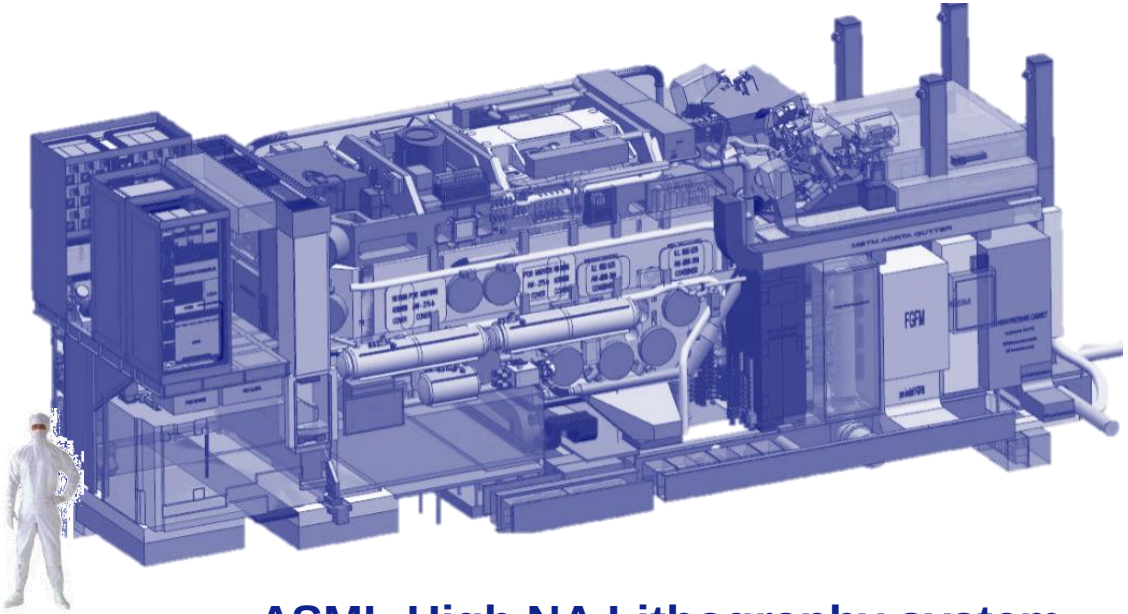


EUV 0.55 NA

High NA introduction at 3nm

[1] TPut: Throughput upgrade (wph)

In the same way 0.33NA enables 7nm Logic, 0.55NA EUV enables 3nm Logic



ASML High NA Lithography system

Process simplification and improved device performance

>> 50% cost reduction compared to multi-patterning schemes

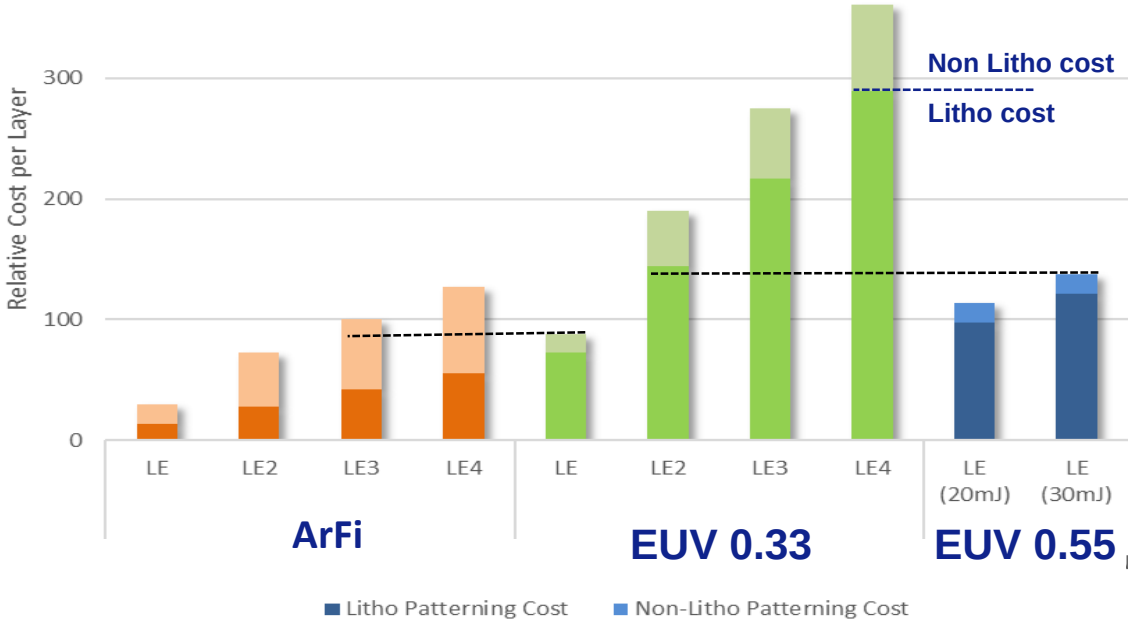
3 to 6x cycle time reduction compared to multi-patterning for critical layers

Best in class overlay performance and focus performance

We have received High NA commitment from 3 customers, for a total up to 12 systems

In the same way 0.33NA enables 7nm Logic, 0.55NA EUV enables 3nm Logic

Total patterning cost comparison: ArFi, EUV 0.33, EUV 0.55



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High NA system design completed, solid progress to support optics development and manufacturing

High NA optics metrology vessels installed in cleanroom @ Zeiss SMT

image removed

Proto High NA mirror

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Forward Looking Statements

This document contains statements relating to certain projections, business trends and other matters that are forward-looking, including statements with respect to expected trends and outlook, strategy, bookings, expected financial results and trends, including expected sales, EUV revenue, gross margin, capital expenditures, R&D and SG&A expenses, cash conversion cycle, and target effective annualized tax rate, and expected financial results and trends for the rest of 2018 and 2019, expected revenue growth and demand for ASML's products in logic and memory, expected annual revenue opportunity in 2020 and for 2025 and expected EPS potential in 2020 with significant growth in 2025, expected trends in the lithography system market, fab capacity by segment, the automotive and artificial intelligence industries, connectivity, semiconductor end markets and new semiconductor nodes, expected acceleration of chipmakers' performance for the next decade, expected EUV insertion and transistor density growth, trends in DUV systems revenue and Holistic Lithography and installed based management revenues, statements with respect to expectations regarding future DUV sales, including composition, margins, improvement of operations and performance, DUV product roadmaps, expected benefits of the holistic productivity approach, including in terms of wafers per year, expected industry trends and expected trends in the business environment, statements with respect to customer demand and the commitment of customers to High NA machines and to insert EUV into volume manufacturing by ordering systems, expected future operation of the High NA joint lab, statements with respect to holistic lithography roadmaps and roadmap acceleration, including the introduction of higher productivity systems in 2019 (including the expected shipment of NXE:3400C and expected timing thereof) and the expected benefits, ASML's commitment to volume manufacturing and related expected plans until 2030, ASML's commitment to secure system performance, shipments, and support for volume manufacturing, including availability, timing of and progress supporting EUV ramp and improving consistency, productivity, throughput, and production and service capability enabling required volume as planned, including expected shipments, statements with respect to growth of fab capacity driving demand in lithography systems, planned customer fabs for 200 systems and expected first output in 2019, expected EUV value increase and increase in EUV margins and ASML's expectation of EUV profitability at the DUV level, expected installed base of EUV systems, expected customer buildout of capacity for EUV systems, EUV estimated demand by market, expected increase in lithography intensity, statements with respect to the expected benefits of EUV, including year-on-year cost reduction and system performance, and of the introduction of the new DUV system and expected demand for such system, the expected benefits of HMI's e-beam metrology capabilities, including the expansion of ASML's integrated Holistic Lithography solutions through the introduction of a new class of pattern fidelity control, the extension of EUV to enable cost effective single patterning shrink with EUV, statements with respect to ASML's applications business, including statements with respect to expected results in 2018, expected growth of the applications business and expected drivers of growth, expected growth in margins, continued shrink and drivers, and expected accuracy, defect control and performance improvements, shrink being a key driver supporting innovation and providing long-term industry growth, lithography enabling affordable shrink and delivering value to customers, DUV, Holistic Lithography and EUV providing unique value drivers for ASML and its customers, expected industry innovation, the expected continuation of Moore's law and that EUV will continue to enable Moore's law and drive long term value for ASML beyond the next decade, intention to return excess cash to shareholders through stable or growing dividends and regularly timed share buybacks in line with ASML's policy, statements with respect to the expectation to continue to return cash to shareholders through dividends and share buybacks, and statements with respect to the expected impact of accounting standards. You can generally identify these statements by the use of words like "may", "will", "could", "should", "project", "believe", "anticipate", "expect", "plan", "estimate", "forecast", "potential", "intend", "continue", "targets", "commits to secure" and variations of these words or comparable words. These statements are not historical facts, but rather are based on current expectations, estimates, assumptions and projections about the business and our future financial results and readers should not place undue reliance on them.

Forward-looking statements do not guarantee future performance and involve risks and uncertainties. These risks and uncertainties include, without limitation, economic conditions, product demand and semiconductor equipment industry capacity, worldwide demand and manufacturing capacity utilization for semiconductors, including the impact of general economic conditions on consumer confidence and demand for our customers' products, competitive products and pricing, the impact of any manufacturing efficiencies and capacity constraints, performance of our systems, the continuing success of technology advances and the related pace of new product development and customer acceptance of and demand for new products including EUV and DUV, the number and timing of EUV and DUV systems shipped and recognized in revenue, timing of EUV orders and the risk of order cancellation or push out, EUV production capacity, delays in EUV systems production and development and volume production by customers, including meeting development requirements for volume production, demand for EUV systems being sufficient to result in utilization of EUV facilities in which ASML has made significant investments, potential inability to successfully integrate acquired businesses to create value for our customers, our ability to enforce patents and protect intellectual property rights, the outcome of intellectual property litigation, availability of raw materials, critical manufacturing equipment and qualified employees, trade environment, changes in exchange rates, changes in tax rates, available cash and liquidity, our ability to refinance our indebtedness, distributable reserves for dividend payments and share repurchases, results of the share repurchase plan and other risks indicated in the risk factors included in ASML's Annual Report on Form 20-F and other filings with the US Securities and Exchange Commission. These forward-looking statements are made only as of the date of this document. We do not undertake to update or revise the forward-looking statements, whether as a result of new information, future events or otherwise.

ASML