SiliconBlue Technologies Corp.

A Lattice Semiconductor Company

iCE65 Family
Ultra Low-Power FPGA
Device Qualification Report

QR 1001

Rev 20110620

1 Purpose

To qualify the product family of iCE65L08, iCE65L04, iCE65P04 and iCE65L01 Ultra Low-Power FPGA with VFBGA package (CB284, CB196, CB132, CB121 and CB81), TQFP (VQ100) and QFN package as well as WLCSP in proven high volume 65nm low power CMOS technology process.

2 Qualification Scope

This qualification plan covers all the products listed below.

- iCE65L01F-CB132
- iCE65L01F-CB121
- iCE65L01F-CB81
- iCE65L01F-VQ100
- iCE65L01F-QN84
- iCE65L01F-DI
- iCE65L01F-CS36
- iCE65L04F-CB284
- iCE65L04F-CB196
- iCE65L04F-CB132
- iCE65L04F-VQ100
- iCE65L04F-DI
- iCE65L04-CS63
- iCE65P04-CB284
- iCE65P04-CB196
- iCE65P04-CB121
- iCE65P04-DI
- iCE65L08F-CB284
- iCE65L08F-CB196
- iCE65L08F-CB132
- iCE65L08F-DI
- iCE65L08F-CC72

- iCE65L08F-CS110

CB284 package was selected as the Product Qualification vehicle. CB196, CB132 and other CB packages in the series are qualified by extension. The same data also qualified Know Good Die (DI) products. Also, by extension, the iCE65L01F product is qualified by the same data.

The VQ and QN packages require Package Qualifications tests (Preconditioning, HAST, Temperature Cycle and High Temperature Storage). Both packages pass all the required qualification tests.

iCE65P04 is qualified via CB284 package.

Our WLCSP product family consists of L08-CC72, L04-CS63, L08-CS110 and L01-CS36. We use CS63 as the Qualification Vehicle. Additional test will be performed as required for CC72 and CS110.

3 Component Information

3.1	General Silicon Info	Values/Comments
	Datasheet	Refer to www.siliconbluetech.com
	Silicon Fab	TSMC, Taiwan
	Wafer Diameter	12 in
	Technology	65nm LP process
	Die Size	L01= 2.49 mm x 2.52mm L04 = 3.83 mm x 3.16 mm L08 = 4.77 mm x 4.35 mm P04= 3.83 mm x 3.08 mm
	Die Thickness	4 Mil
	# of Metal Layers	8 + Al Pad
	# of Poly Layers	1

3.2	**Package Assembly Process**	
	Assembly Flow Chart	Per ASE's assembly flow
	Locations	ASE, Taiwan / ASE, Malaysia
	Subcon	ASE, Taiwan / ASE Malaysia

3.3 SiliconBlue Technologies iCE65 product silicon fabrication description.

The generic process is TSMC 65nm CMOS logic low power purpose at 1 .2/2.5V of 1P8M option with copper interconnect and low-K dielectric (hereafter 65LP). Core devices operate at 1.2V. I/O devices operate at 2.5V with an overdrive option to 3.3V plus 5V-Tolerant. The qualification results were obtained from Fab 12. Same specifications are applied to 65LP generic process released by other manufacturing fab in TSMC.

To guarantee SiliconBlue Technologies products manufactured by TSMC generic process with good reliability, the process qualification items and specifications are defined and executed. The TSMC qualification methods, requirements and results are summarized in this document.

Process qualification consists of reliability tests listed below. The test vehicle structures, sample size, stress conditions, failure criteria, specifications and test results for 65LP process are detailed in Appendix A.

All the tests passed with no failures detected.

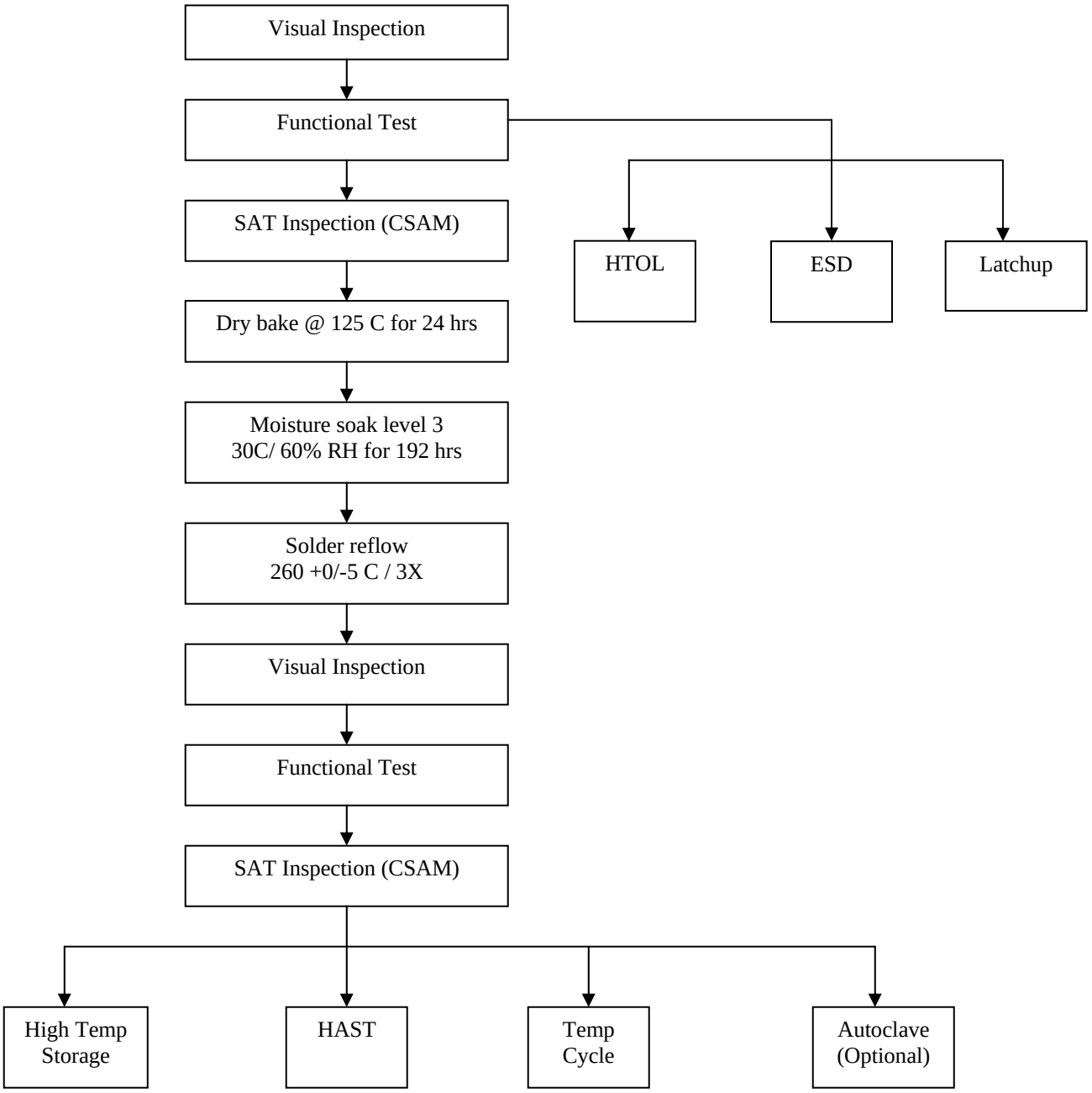
Tests List:

1. Gate oxide VBD
    - To evaluate the gate oxide quality and determine its defect density
    - Oxide breakdown voltage is measured
2. Gate oxide time-dependent dielectric breakdown (TDDB)
    - To predict gate oxide life time under normal operation
    - Time to oxide breakdown is measured
3. Plasma process induced damage (PID)
    - To monitor charging damage to gate oxide caused at all process steps
    - Antenna structures ratio for poly, contact, via and metal larger than design

rules to increase sensitivity

4. Hot carrier injection (HCI)
    - To evaluate the hot carrier effect of MOSFET and predict the life time under normal operation
5. Negative bias temperature instability (NBTI)
    - To predict PMOS lifetime under negative bias stress at high temperature
    - Idsat degradation is monitored.
6. Electromigration (EM)
    - To evaluate the quality of metallization process and determine the lifetime, current density and failure rate of metal interconnects, via, stack via and contact under normal operation conditions
    - Resistance changes of metal and via interconnects are monitored
7. Stress migration (SM)
    - To evaluate the quality of via and stacked via chains against thermal stress condition
    - Resistance changes are monitored
8. IMD low-K time dependent dielectric breakdown (IMD low-k TDDB)
    - To evaluate the quality of low-k dielectric inter-metal layers and determine the lifetime under normal operation conditions
    - Leakage current changes of inter-metal and intra-metal/via test structures are monitored

4 Product Reliability Test Flow



5. Qualification Requirement

SiliconBlue Technologies Corporate specification ENG_103 requires exhaustive reliability testing of a new product prior to mass production. This insures that intrinsically reliable product gets shipped to the customer. While this rigorous reliability qualification activity can prove to be costly and time consuming, it serves to minimize the customer's component qualification burden. SiliconBlue Technololgies makes these results available to the customer.

The table listed below defines the reliability tests that need to be performed:

Test	Conditions	Test Method	No. of Lots	Sample Size/Lot	Acceptance Criteria
ESD (HBM)	Characterization above and below 2000 V DC, using Human Body Model (HBM)	EIA/JESD22-A114	2	3	+/- 2000V
ESD (MM)	Characterization above and below 200 V DC, using Machine Model	EIA/JESD22-A115	2	3	+/- 200V
ESD (CDM)	Characterization above and below 1000 V DC, using Charge Device Model (CDM)	EIA/JESD22-C101	2	3	+/- 1000V
Latch Up (LU)	Characterization for latch-up sensitivity	EIA/JESD78	2	6	+/- 100mA
Preconditioning	All units subject to TC, HAST, T/C, and HTS: dry bake, Moisture Level 3, 3x solder reflow, Sampling CSAM performed pre/post Preconditioning	JESD22-A113	NA	NA	LTPD: 1
HTOL (early Life)	168hours at 125 C ambient dynamic operation	EIA/JESD22-A108	3	77	< 70 FITs
HTOL (extended)	1000hrs at 125 C ambient dynamic operation	EIA/JESD22-A108	3	77	< 50 FITs
Temperature Cycle (TC)	-700 cycles at –55 C to 125 C static operation;	JESD22-A104	3	25	≤ 2 failures
Biased HAST	- 96 hours at 130 C and 85 RH dynamic operation.	JESD22-A110	3	25	≤ 2 failures
High Temp Storage (HTS)	- 1000hr @ 150C	JESD22-A-103	3	77	0 failure

6 Qualification Summary

A. L08/L04/L01 CB Data - Pass

Test	Device	Lot#	Qty	# of Rejects
Temp Cycle	iCE65L04F-CB284	Lot #1	25	0
	iCE65L08F-CB284	Lot #2	25	0
	iCE65L04F-CB284	Lot #3	25	0
	iCE65L08F-CB284	Lot #4	25	0
High Temp Storage	iCE65L04F-CB284	Lot #1	77	0
	iCE65L08F-CB284	Lot #2	77	0
	iCE65L04F-CB284	Lot #3	77	0
	iCE65L08F-CB284	Lot #4	77	0
HTOL (Early life & Extended Life)	iCE65L04F-CB284	Lot #1	77	0
	iCE65L08F-CB284	Lot #2	77	0
	iCE65L04F-CB284	Lot #3	77	0
	iCE65L08F-CB284	Lot #4	77	0
	iCE65L04F-CB284	Lot #5	77	0
	iCE65L04F-CB284	Lot #6	77	0
HAST	iCE65L04F-CB284	Lot #1	25	0
	iCE65L08F-CB284	Lot #2	25	0
	iCE65L04F-CB284	Lot #3	25	0
	iCE65L08F-CB284	Lot #4	25	0
Preconditioning	iCE65L04F-CB284	Lot #1	77	0
	iCE65L08F-CB284	Lot #2	77	0
	iCE65L04F-CB284	Lot #3	77	0
	iCE65L08F-CB284	Lot #4	77	0

Test				Pass Limits
ESD HBM	iCE65L04F-CB284	Lot #1	3	+/- 2000V
	iCE65L08F-CB284	Lot #2	3	+/- 2000V
ESD MM	iCE65L04F-CB284	Lot #1	3	+/- 200V
	iCE65L08F-CB284	Lot #2	3	+/- 200V
ESD CDM	iCE65L04F-CB284	Lot #1	3	+/- 2000V
	iCE65L08F-CB284	Lot #2	3	+/- 2000V
Latch-up	iCE65L04F-CB284	Lot #1	6	+/- 100mA @ 85C
	iCE65L08F-CB284	Lot #2	6	+/- 100mA @ 85C

B. L04/L01 VQ100 Data - Pass

Test	Device	Lot#	Qty	# of Rejects
Preconditioning	iCE65L04F-VQ100	Lot #1	150	0
Temp Cycle	iCE65L04F-VQ100	Lot #1	25	0
HTS	iCE65L04F-VQ100	Lot #1	25	0
HAST	iCE65L04F-VQ100	Lot #1	25	0
Test				Pass Limits
ESD (CDM)	iCE65L04F-VQ100	Lot #1	3	+/- 1000V
Latch up	iCE65L04F-VQ100	Lot #1	6	+/- 100mA @ 85C

C. L08/L04/L01 CS Data - Pass

Test	Device	Lot#	Qty	# of Rejects
HTOL (Early life & Extended Life)	iCE65L04F-CS63	Lot#1	75	0
		Lot#2	77	0
		Lot#3	77	0
Preconditioning	iCE65L04F-CS63	Lot #1	140	0
		Lot#3	150	0
Temp Cycle	iCE65L04F-CS63	Lot #1	45	0
		Lot#3	45	0
HAST	iCE65L04F-CS63	Lot #1	25	0
		Lot#3	25	0
HTS	iCE65L04F-CS63	Lot #1	25	0
		Lot#3	25	0
Auto Clave [JEDEC22-A102]	iCE65L04F-CS63	Lot #1	44	0
		Lot#3	45	0
Test				**Pass Limits**
ESD CDM	iCE65L04F-CS63	Lot #1	3	+/-2000V
		Lot#3	3	+/-2000V

D. QN Data - Pass

Test	Device	Lot#	Qty	# of Rejects
Preconditioning	iCE65L01F-QN84	Lot #1	150	0
Temp Cycle	iCE65L01F-QN84	Lot #1	25	0
HAST	iCE65L0F-QN84	Lot #1	25	0
Auto Clave [JEDEC22-A102]	iCE65L01F-QN84	Lot #1	45	0
HTS	iCE65L01F-QN84	Lot#1	25	0
Test				**Pass Limits**
ESD CDM	iCE65L01F-QN84	Lot #1	3	+/- 2000V

E. P04 CB Data - Pass

Test	Device	Lot#	Qty	# of Rejects
HTOL (Early life & Extended Life)	iCE65P04-CB284	Lot #1	80	0
Test				**Pass Limits**
ESD (CDM) (All pins except AVDD pin)	iCE65P04-CB284	Lot #1	3	+/- 2000V
ESD (CDM) (AVDD pin only)	iCE65P04-CB284	Lot #1	3	+/- 1000V
ESD(MM) (All pins except AVDD pin)	iCE65P04-CB284	Lot #1	3	+/-200V

ESD(MM) (AVDD pin only)	iCE65P04-CB284	Lot #1	3	+/-100V
ESD (HBM) (All pins except AVDD pin)	iCE65P04-CB284	Lot #1	3	+/-1000V
ESD (HBM) (AVDD pin only)	iCE65P04-CB284	Lot #1	3	+/-500V
Latch up	iCE65L04F-VQ100	Lot #1	6	+/- 100mA @ 85C

Note :

All HTOL qualification parts on every lot has high % utilization reliability pattern programmed into the One Time Programmable array (NVCM) and burn-in throughout the life test. All bits are verified for integrity at every read point during the life test.

Total programmed bit life test hour: L04 = 16,170 Mbit-hour
L08 = 32,340 Mbit-hour

Result: 0 Failure

7 Revision History

20090720	Initial release
20090830	Rewrite the report in standard report format
20091030	Update with Fab Rel data
20100315	Update with New Rel data
20100409	Update with New Rel Data
20100430	Update with New Rel Data
20100604	Update with New Rel Data
20100901	Update with New Rel Data
20110418	Update with New Rel Data
20110418A	Minor Typo correction
20110618	Update Report Title
20110620	Correct CS data table

Qual Items	DUT	Structures	Sample size	Stress Conditions	Failure Criteria	Specifications	Result
Gate oxide VBD	1.2V Core	Area = 5e2 ~ 2.4e3 um^2	>=3 wafer/lot; 3 lots; 25,560	Voltage ramp 3.3V/s (inversion mode)	Ig leak > 40uA @ 1V	Do <= 5/cm^2 @ VBD <= 1.2V Do <= 1/cm^2 @ 1.2V < VBD < 2.9V	**Pass**
	2.5V I/O	Area = 4.8e3 ~ 1e6 um^2		Voltage ramp 6.27V/s (accumlation mode)	Ig leak > 15uA @ 1.5V	Do <= 5/cm^2 @ VBD <= 2.5V Do <= 1/cm^2 @ 2.5V < VBD < 5.0V	**Pass**
	2.5V I/O over drive			Voltage ramp 6.27V/s (accumlation mode)	Ig leak > 15uA @ 1.5V	Do <= 5/cm^2 @ VBD <= 3.3V Do <= 1/cm^2 @ 3.3V < VBD < 7.2V	**Pass**
Gate oxide TDDB	1.2V Core	Area ~ 1e7 um^2 (W/L=1/0.06)	>= 50/stress/lot; 3 lots	3-5 stress voltage @ 125C & field ~ 8-12MV/cm	1st soft breakdown	TTF @0.1% cum failure rate > 10yr for 0.1cm^2 @ 125C & 1.2V+10%	**Pass**
	2.5V I/O	Area ~1e6 um^2 (W/L=4/4.8 x 2000)		3-5 stress voltage @ 125C & field ~ 8-12MV/cm	Hard breakdown	TTF @0.1% cum failure rate > 10yr for 0.01cm^2 @ 125C & 2.5V+10%	**Pass**
	2.5V I/O over drive			3-5 stress voltage @ 125C & field ~ 8-12MV/cm	Hard breakdown	TTF @0.1% cum failure rate > 10yr for 0.01cm^2 @ 125C & 3.3V+10%	**Pass**
PID	1.2V Core	W/L=5/0.2	>= 4 wafer/lot; 3 lots	Ig @Vg=1.4Vcc inversion	Ig tailing	Ig tailing < 5%	**Pass**
	2.5V I/O	W/L=2.63/0.38		Ig @Vg=1.8Vcc (2.6Vcc) for NMOS (PMOS)			
HCI	1.2V Core	W/L=1/0.06	24/pattern/lot; 3 lots	1.2V (Vds=Vgs=1.7V, 1.8V, 1.9V, 2.0V) TTF vs 1/Vds	Idsat change > 10%	DC liftetime > 0.2 yr	**Pass**
	2.5V I/O	W/L=10/0.28	15/pattern/lot; 3 lots	2.5V (Vds=3.3V, 3.5V, 3.7V, Vgs@Isub(max)) TTF vs $Isub^{-m}$		AC lifetime > 10 yr	**Pass**
	2.5V I/O over drive	W/L=10/0.5 (N), 10/0.4 (P)		2.5V (Vds=4.1V, 4.3V, 4.5V, Vgs@Isub(max)) TTF vs $Isub^{-m}$		0.1% cum failure @25C, Vcc+10% (Core P @125C)	**Pass**
NBTI	1.2V Core	W/L=1/0.06	>= 20/lot; 3 lots	Vg: 6-9 MV/cm @ 125C; Vs=Vd=Vb=grounded	Idsat degrade > 10%	TTF 0.1% cum failure @125C, Vcc+10% >5 yr	**Pass**
	2.5V I/O	W/L=10/0.28					
	2.5V I/O over drive	W/L=10/0.4					
EM	M1 + contact	W/S=0.09/0.09 (1800 A)	> 20/pattern/lot; 3 lots	Jstess=1-5MA/cm^2 @ 300C	dR >10% Ro	TTF 0.1% cum failure @110C > 100k hr	**Pass**
	Mx + Vx	W/S=0.10/0.10 (2200 A)					
	My + Vy	W/S=0.20/0.20 (5000 A)		Jstess=1-5MA/cm^2 @ 350C			
	Al-Cu RDL	W/S=3/2 (14.5K A)		Jstess=1-5MA/cm^2 @ 250C			
SM	Vias chain	metal-via overlap from min to 0.7	>130/lot; 3 lots	500 hr bake @175C	dR >10% Ro	No failure allowed	**Pass**
IMD Low-K TDDB	M1, V1, M2 combs	M1 & M2 W/S=Min/Min V1 W/S=0.10/0.13	>30 /pattern/lot; 3 lots	2.5-4.0 MA/cm @ 125C	I(TBD) = 100 x I(T=0)	TTF 0.1% cum failure @125C & 3.6V > 10 yr	**Pass**