ORCA® Series 4 FPGA PLL Elements

September 2004 Technical Note TN1014

Introduction

The *ORCA* Series 4 FPGA platform has been designed for the delivery of networking IP, with improved performance and decreased time-to-market.

To facilitate the feature-rich, high-speed architecture of the Series 4, and to support the fast-paced networking markets, fixed and programmable phase-locked loop (PLL) components have been embedded in each Series 4 array. There are a total of eight PLL components in each Series 4 FPGA, with six being programmable and two that are fixed. PLLs have analog circuits based on voltage controlled oscillators (VCO) and phase/frequency detectors (PFD) that compare the frequency and phase of two input signals. This analog circuit provides for maximum performance and flexibility and also acts as a filter on the PLL input clock to attenuate high-frequency jitter. With Series 4 FPSCs, there are four programmable PLLs in the FPGA portion of the device.

Some of the capabilities of PLLs include automatic delay compensation, clock frequency multiplication, clock frequency division, duty cycle modifications, and clock phase modification.

PLL Types

There are four types of PLL elements in the generic *ORCA* Series 4 FPGA devices; these are indicated in Table 1. Following Table 1 are details for each type with a description, pinout, and specifications.

Table 1. Series 4 PLL Types

PLL Type	Qty	Description	Frequency Range
PLL1	1	Dedicated T1/E1 PLL	1 MHz or 2 MHz
PLL2	1	Dedicated STS-3 PLL OC-3/STM-1	140 MHz—170 MHz
PPLL	4	Programmable PLL	15 MHz—200 MHz
HPPLL	2	High-speed programmable PLL	60 MHz—420 MHz

Dedicated PLL Descriptions

Figure 1. PLL1 Element

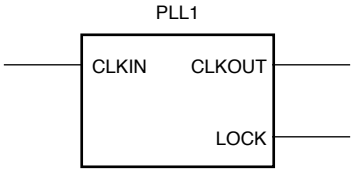
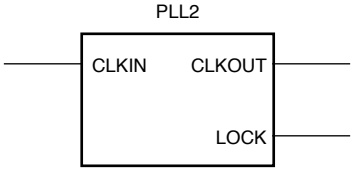


Figure 2. PLL2 Element



The Series 4 family of FPGAs includes two dedicated PLL elements, PLL1 and PLL2. These two PLLs are designed with telecom clocking in mind and thus have a narrow input and output frequency ranges. One characteristic of these dedicated PLLs is their low jitter transfer values, which allow them to filter a significant amount of the input jitter. The operation and use of these PLLs is described below.

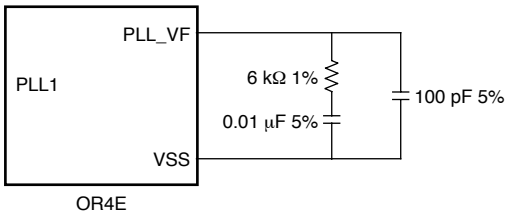
PLL1

PLL1 is a dedicated phase-locked loop (PLL) intended for clock conditioning at 1.544 MHz or 2.048 MHz (T1/E1 line transmission rates). This PLL generates an ultraclean, near-perfect output clock from an imperfect input clock and a lock signal indicating that the PLL is locked to the input clock reference. Figure 1 reflects the PLL1 element and its associated input and output pins.

Proper operation of PLL1 requires the addition of an external low-pass filter. This external filter is necessary to achieve the low noise capabilities of the PLL. Three external passive components R, C1, and C2 make-up the low-pass filter with the values shown in Figure 3. Proper board layout techniques should be employed when placing external components to avoid degradation of filter performance. Table 2 shows the dedicated PLL filter pins (PLL_VF) for each package offering. External filter connections should only be made to these dedicated pins. PLL1 is not available in FPSCs based on the Series 4 architecture.

Note: When designing with PLL1, the user is required to select the dedicated PLL1 clock input pins to gain access to PLL1. These dedicated PLL clock input pins are shown in Table 5.

Figure 3. PLL1 External Filter



To achieve the low noise requirement of the board design, the low-pass filter must be connected to the dedicated PLL filter pins for each of the BGA packages as shown in Table 2.

Table 2. . BGA Ball Names of PLL_VF and Dedicated Vss

Package Name	256 PBGA	352 PBGA	416 PBGAM	432 EBGA	680 PBGAM
PLL_VF Ball Name	B14	B24	B24	C4	D30

PLL2

PLL2 is a dedicated phase-locked loop (PLL) intended for clock conditioning at 155.52 MHz (STS-3/OC-3/STM-1 line transmission rate). This PLL generates an ultraclean, near-perfect clock from an imperfect input clock and a lock signal indicating that the PLL is locked to the input clock.

No external filter is required for the use of PLL2; however, the dedicated clock input pins in Table 5 must be used to access this PLL. Figure 2 reflects the PLL2 element and its associated input and output pins. PLL2 is not available in FPSCs based on the Series 4 architecture.

Note: When designing with PLL2, the user is required to select the dedicated PLL2 input pins to be used to gain access to PLL2. These dedicated PLL input pins are shown in Table 5 below.

Table 3 shows the electrical specifications for the dedicated PLL1 and PLL2 elements.

Table 3. PLL1 and PLL2 Specifications

Parameter	PLL1			PLL2			Unit
	Min	Nom	Max	Min	Nom	Max	
VDD15	1.425	1.5	1.575	1.425	1.5	1.575	V
VDD33	3.0	3.3	3.6	3.0	3.3	3.6	V
Operating Temperature	–40	—	125	–40	—	125	˚C
Input Duty Cycle	30	—	70	30	—	70	%
Input Rise/Fall Time	—	—	5	—	—	5	ns
Input Clock Jitter Requirement*	—	—	0.10	—	—	0.05	UIp-p
Input Jitter Transfer†	—	—	8.0	—	—	5.0	%
Input Clock Frequency	1.0	—	2.5	140	155.52	170	MHz
Output Clock Frequency	1.0	—	2.5	140	155.52	170	MHz
Output Duty Cycle	47	50	53	47	50	53	%
dc Power Consumption	—	20	—	—	50	—	mW
Total On Current (dc)	—	2.5	—	—	2.4	—	mA
Total Off Current (dc)	—	40	—	—	30	—	pA
Cycle to Cycle Jitter (p-p)‡	—	—	0.010	—	—	0.020	UIp-p
Period Jitter (p-p)§	—	—	0.010	—	—	0.020	UIp-p
Duty Cycle Jitter (p-p)**	—	—	0.005	—	—	0.025	UIp-p
Lock Time	—	<1200	—	—	<50	—	μS

* The Input Clock Jitter Requirement is a maximum value that allows the PLL to operate properly. Uip-p is Unit Interval peak-peak. A UI is equal to one clock period. Reduced values of input jitter lead directly to improved output jitter. Values are 6 sigma results.

† Input Jitter Transfer is the percentage of the jitter at the input of the PLL that is transferred to the output of the PLL. Unlike a delay-locked loop (DLL), a PLL can filter some of the input jitter. Values are 6 sigma results.

‡ Cycle to Cycle Jitter is the min/max measurement of the time between successive rising edges. This value does not include the input jitter, a percentage of which must be added to this value to obtain the total output jitter. Values are 6 sigma results based on the UI at the PFD inputs.

§ Period Jitter is the min/max measurement of the time when all rising edges occur versus the ideal edge locations. This value does not include the input jitter, a percentage of which must be added to this value to obtain the total output jitter. This value is typically used to determine the worst-case clock period for full-cycle transfers inside the device and when interfacing to other components. Values are 6 sigma results based on the UI at the PFD inputs.

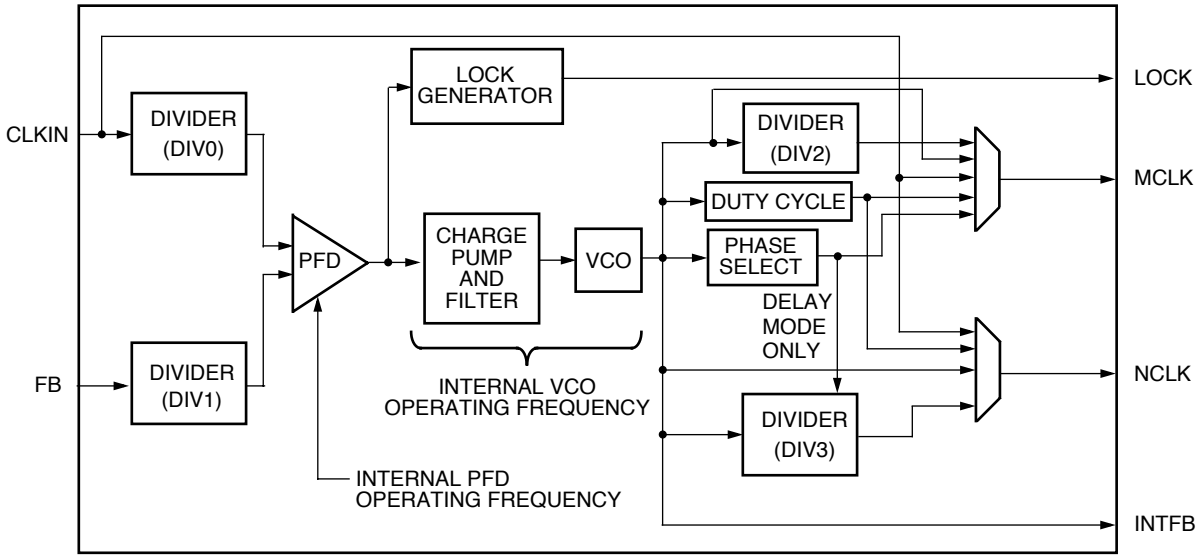
** Duty Cycle Jitter is the min/max measurement of the time between successive rising to falling edges, or falling to rising edges. This value does not include the input jitter, a percentage of which must be added to this value to obtain the total output jitter. This value is used to determine the worst-case clock period for half-cycle data transfers. Values are 6 sigma results based on the UI at the PFD inputs.

Note:For PLL1 and PLL2, the input clock frequency, the output clock frequency, the PFD clock frequency and the VCO clock frequency always run at the same rate.

Programmable PLL Descriptions

Figure 4 shows the structure of both types of programmable PLLs found in Series 4 FPGAs and FPSCs.

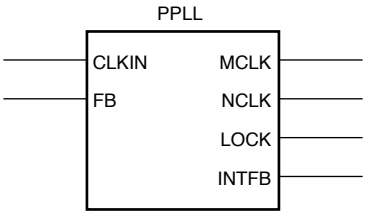
Figure 4. Programmable PLL Detailed Structure



PPLL

PPLL is a programmable phase-locked loop (PPLL) for frequency multiplication/division and phase and duty cycle adjustment. This PLL features a pair of programmable output clocks (MCLK and NCLK) from one input clock. See "Programmable PLL Attributes" on page 8. for details on how to control the frequency multiplication/division and phase and duty cycle adjustment. This element also generates a lock signal (LOCK) indicating that the PLL is locked to the input clock. The FB pin is used to input the clock feedback. This pin must always be connected, and the internal feedback (INTFB) is provided to connect to FB if no external feedback is desired. Figure 5 reflects the PPLL element and its associated input and output pins.

Figure 5. PPLL Element



HPPLL

HPPLL is a high-speed programmable phase-locked loop (HPPLL) for frequency multiplication/division and phase and duty cycle adjustment. This PLL features a pair of programmable output clocks from one input clock. See Programmable PLL Attributes for details on how to control the frequency multiplication/division and phase and duty cycle adjustment. This element also generates a lock signal indicating that the PLL is locked to the input clock and it also contains FB and INTFB pins. Figure 6 reflects the HPPLL element and its associated input and output pins.

Figure 6. HPPLL Element

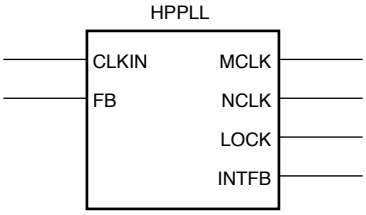


Figure 4 shows the specifications for the PPLL and HPPLL elements.

Table 4. PPLL and HPPLL Specifications

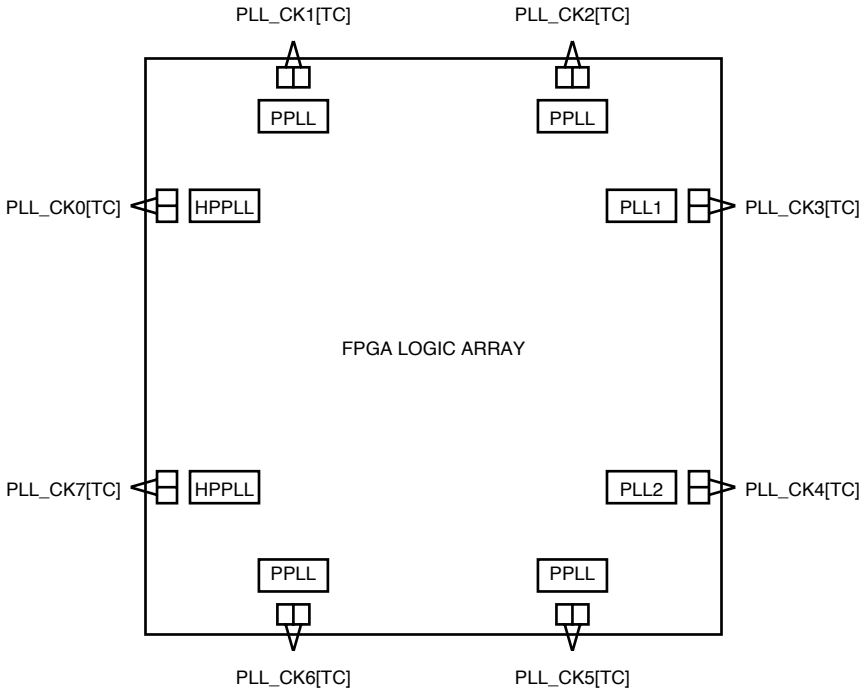
Parameter	PPLL			HPPLL			Unit
	Min	Nom	Max	Min	Nom	Max	
VDD15	1.425	1.5	1.575	1.425	1.5	1.575	V
VDD33	3.0	3.3	3.6	3.0	3.3	3.6	V
Operating Temperature	–40	—	125	–40	—	125	˚C
Input Clock Frequency	15	—	200	60	—	420	MHz
Input Duty Cycle	30	—	70	30	—	70	%
Input Rise/Fall Time	—	—	5	—	—	5	ns
Input Jitter Transfer[1]	—	—	15.0	—	—	20.0	%
Input (PFD) Clock Frequency	2.0	—	200	7.5	—	420	MHz
Output (VCO) Clock Frequency	15	—	200	60	—	420	MHz
MCLK and NCLK Output Frequency	2.0	—	200	7.5	—	420	MHz
Output Duty Cycle	45	50	55	45	50	55	%
dc Power Consumption	—	28	—	—	50	—	mW
Total On Current (dc)	—	8.5	—	—	14	—	mA
Total Off Current (dc)	—	30.0	—	—	30.0	—	pA
Cycle to Cycle Jitter (p-p)[1, 4]	—	—	0.020	—	—	0.020	UIp-p
Period Jitter (p-p)[1, 4]	—	—	0.015	—	—	0.015	UIp-p
Duty Cycle Jitter (p-p)[1, 4]	—	—	0.025	—	—	0.025	UIp-p
M Output vs. N Output Jitter[3, 4]	—	—	20	—	—	20	ps
Lock Time	—	<50	—	—	<50	—	μS
Frequency Multiplication[2]	1x, 2x, 3x, 4x, 5x, 6x, 7x, 8x, others to 64x						—
Frequency Division[2]	1/8x, 1/7x, 1/6x, 1/5x, 1/4x, 1/3x, 1/2x, others to 1/64x						—
Duty Cycle Adjust of Output Clock(s)	12.5, 25, 37.5, 50, 62.5, 75, 87.5						%
Delay Adjust of Output Clock	0, 45, 90, 135, 180, 225, 270, 315						degrees
Phase Shift Between MCLK and NCLK	0, 45, 90, 135, 180, 225, 270, 315						degrees

Notes:
1. See Table 3 for an explanation of these jitter values.
2. Combinations of frequency division and frequency multiplication are valid for each PLL output ([1:8][1:8] / [1:8][1:8]).
3. M output vs N output jitter is the worst case relationship between these two outputs from the PLL when they are programmed to have the same phase.
4. UIp-p values are based on the MCLK and NCLK output frequencies. For VCO frequencies of 15 MHz to 25 MHz for the PPLL element, the Cycle to Cycle Jitter (p-p) = 0.030 UIp-p, the Period Jitter (p-p) = 0.025 UIp-p, and the Duty Cycle Jitter = 0.035 UIp-p.

PLL Locations and Access

There are a total of eight (8) PLLs in each of the Series 4 FPGA devices: one PLL1, one PLL2, two HPPLLs, and four PPLLs. The PLLs are located two each in the corners of the array and are shown in Figure 7. Each PLL has two dedicated external input pins for the clock inputs, allowing for differential clocks (LVPECL or LVDS). In Figure 7, the T or C labels indicate true and complement pins for a differential input buffer. When using single-ended buffers, designers should use the true clock input pin.

Figure 7. PLL and PLL Input Pin Locations



PLL Power Supply

The PLLs on *ORCA* Series 4 devices all operate from the $V_{DD}33$ power supply. Care needs to be taken during board layout to isolate and filter this power supply from all other power supplies to ensure proper PLL operation. The power supply filtering is in the form of:

- A parallel bypass capacitor network consisting of 10 μF, 0.1 μF, and 1.0 μF capacitors close to the power source.
- A parallel bypass capacitor network consisting of 0.01 μF and 0.1 μF close to each pair of programmable PLLs on the FPGA or FPSC (four networks for FPGAs and two networks for FPSCs).

PLL Pin/Component Locations

PLLs can have their CLKIN input driven by any signal, including those generated inside the device. Although any I/O pin can drive the PLL CLKIN signal, the primary clock inputs and the semi-dedicated PLL inputs should be used to reduce overall jitter and clock injection time when possible.

Table 5 shows the input pin names as well as the PLL type and PLL name for each of the PLLs across the three package offerings for Series 4 FPGAs. Consult each FPSC data sheet for their PLL pin locations. There are two types of PLLs: PPLL and HPPLL. In the naming convention in Table 5 below, the prefix UL, UR, LR, and LL correspond to upper left, upper right, lower right, and lower left, respectively.

For optimum performance, it is recommended that the user lock down the appropriate pins for the selected PLL location as shown in Table 5. This can be done using the LOCATE preference command placed in the design preference file used by ispLEVER (PAR) software, or via constraints set up in the synthesis tool.

In addition to locking down the PLL pins, it is recommended that the desired PLL component be locked or placed as well. This is accomplished by using the LOCATE preference command. Below is an example showing the use of the LOCATE preference to lock a clock signal called MyClkNet to the dedicated PLL input clock pin D6. The PCM component labeled MyPLL is located at the site ULPPLL, which forces the PPLL component to be placed in the upper left side of the FPGA array. See the ispLEVER help system for detailed information with regard to preference file syntax and usage.

For PLL1 and PLL2 the dedicated inputs must be used.

Example

LOCATE COMP "MyClkNet" SITE "D6"; # Locks clock signal MyClkNet to pin D6 in 680 BGA package.

LOCATE COMP "MyPPLL" SITE "ULPPLL";

Table 5. PLL Input Pin Names and Locations

PLL Type	PLL Name	Package Pin Name	Pin Type	256 PBGA	352 PBGA	416 PBGAM	432 EBGA	680 PBGAM
HPPLL	ULHPPLL	PLL_CK 0 T	True	E3	E4	E3	E31	F4
		PLL_CK 0 C	Complement	F5	E2	D2	E30	D1
PPLL	ULPPLL	PLL_CK 1 T	True	E5	A4	D6	D26	C6
		PLL_CK 1 C	Complement	B4	D5	D5	C27	D6
PPLL	URPPLL	PLL_CK 2 T	True	C13	B23	C23	A4	B31
		PLL_CK 2 C	Complement	A14	A24	D22	B4	C30
PLL1	URPLL1	PLL_CK 3 T	True	D14	E24	C26	D1	E31
		PLL_CK 3 C	Complement	C16	C25	B25	D2	G30
PLL2	LRPLL2	PLL_CK 4 T	True	P16	AD26	AD25	AH2	AJ30
		PLL_CK 4 C	Complement	N14	AC25	AD26	AH1	AK32
PPLL	LRPPLL	PLL_CK 5 T	True	T14	AE24	AC22	AK4	AL30
		PLL_CK 5 C	Complement	R14	AD23	AC23	AJ4	AP31
PPLL	LLPPLL	PLL_CK 6 T	True	T3	AF3	AC5	AK28	AN4
		PLL_CK 6 C	Complement	P4	AE4	AD4	AL28	AK7
HPPLL	LLHPPLL	PLL_CK 7 T	True	N3	AC1	AB4	AF28	AK2
		PLL_CK 7 C	Complement	N2	AB4	AA4	AG29	AK1

Note:The True and Complement pin pairs must be used for differential inputs such as LVDS and LVPECL. All single-ended inputs must use only the True input pin.

Programmable PLL Attributes

For the programmable PLLs (PPLL and HPPLL), the frequency multiplication/division, phase, and duty cycle adjustment are controlled by the designer with attributes assigned to the instantiated PLL library elements. These attributes are shown here for reference; ispLEVER Module/IP Manager should be used to generate all PLL HDL modules. A detailed discussion of ispLEVER Module/IP Manager is given below. The programmable PLL attributes and their valid values are show in Table 6.

Table 6. Series 4 PLL Attributes and Valid Values

PLL Attribute	Value
MCLKMODE	BYPASS, DUTYCYCLE, PHSHIFT, DELAY
NCLKMODE	BYPASS, DUTYCYCLE, PHSHIFT, DELAY
VCOTAP	0, 1, 2, 3, 4, 5, 6, 7
DIV0	1, 2, 3, 4, 5, 6, 7, 8
DIV1	1, 2, 3, 4, 5, 6, 7, 8
DIV2	1, 2, 3, 4, 5, 6, 7, 8
DIV3	1, 2, 3, 4, 5, 6, 7, 8
FB_PDEL	DEL0, DEL1, DEL2, DEL3

Note:DIV0, DIV1, DIV2, and DIV3 are the values for dividers as shown in Figure 4.

Attributes

Following is a brief discussion of the attributes listed in Table 6. Discussion and examples of each of the modes for MCLK and NCLK follows below. It is recommended that the user let ispLEVER Module/IP Manager generate all of the attributes listed in Table 6 with the exception of FB_PDEL. This attribute will need to be added by the user.

MCLKMODE and NCLKMODE Attributes

These two attributes control the mode of PLL outputs MCLK and NCLK. The PLL can be in one of four modes: BYPASS, DUTYCYCLE, PHSHIFT, or DELAY. MCLKMODE and NCLKMODE must be set to the same value for each instantiation of the PLL. ispLEVER Module/IP Manager will generate these attributes automatically based on the mode selection chosen when running ispLEVER Module/IP Manager.

VCOTAP Attribute

VCOTAP is a PLL attribute, which controls the amount of phase shift when the PLL is placed in PHSHIFT or DELAY mode. Table 7 shows the valid values of VCOTAP and the corresponding phase shift for each value. ispLEVER Module/IP Manager will automatically generate these attributes based on the mode selection.

Table 7. VCOTAP Phase Shift Values

VCOTAP	Phase Shift (degrees)
0	0
1	45
2	90
3	135
4	180
5	225
6	270
7	315

The VCOTAP attribute is also used to select the output clock duty cycle values when in DUTYCYCLE mode.

DIV0, DIV1, DIV2, and DIV3 Attributes

These attributes control the PLL when in DELAY mode for frequency, multiplication, and division. Valid values are shown in Table 6. The DIV0, DIV1, DIV2, and DIV3 attributes will automatically be set to 1 by ispLEVER Module/IP Manager for all modes other than DELAY mode where frequency multiplication or division is being performed on the input clock. These attributes must be in the HDL code even if the desired mode does not make use of them. The ispLEVER Module/IP Manager will generate these attributes automatically based on the input and output frequency entered.

FB_PDEL Attribute

The FB_PDEL is an attribute that is used to specify a fixed value of feedback delay that is built into the PLL, and may be used in the PPLL and HPPLL elements only. Adding feedback delay to the PLL decreases clock insertion delay, which in turn decreases clock to out but may increase input setup times. Design examples that show the use of FB_PDEL and its resulting effect on clock to out and input setup times are included at the end of this document. Note that these delays are independent to the phase delays generated by the PLLs.

The four values associated with the FB_PDEL attribute are DEL0, DEL1, DEL2, and DEL3. The values for each of these delays are found in the Series 4 data sheet. The FB_PDEL attribute must be manually added to the HDL code generated by ispLEVER Module/IP Manager.

PLL Simulation

When simulating a design containing PLLs, and a global reset is used, it is recommended that the global reset be asserted for no more than two clock cycles. Asserting the global reset for longer than two clock cycles will cause incorrect behavior of the PLL model.

Modes of Operation

The four possible modes for MCLK and NCLK on the PPLL and HPPLL are shown below. Mixing modes between MCLK and NCLK is not recommended. The ispLEVER Module/IP Manager should be used to generate all PLL elements. See the next section for details on running ispLEVER Module/IP Manager.

BYPASS

In BYPASS mode, both outputs MCLK and NCLK are active and may be used by the designer. However, when only one output is used, no additional dedicated clock routing resources are consumed by the unused output. When in BYPASS mode, outputs MCLK and NCLK are equal to the input clock CLKIN and are phase-locked to each other. No delay compensation or duty cycle compensation is done in BYPASS mode, and a delay to the clock route is incurred.

One possible use for BYPASS mode is where a designer may have to perform clock manipulation as design requirements change, and the PLL component needs to be added to the design. Selecting the dedicated PLL clock pins facilitates this consideration and minimizes clock insertion delay.

DUTYCYCLE

In DUTYCYCLE mode, both MCLK and NCLK are active and may be used by the designer. Both MCLK and NCLK will have the same duty cycle adjustment and are copies of the same clock signal. Phase shift is not available for MCLK and NCLK in DUTYCYCLE mode. The value of VCOTAP controls the amount of duty cycle adjustment. Valid values for VCOTAP in DUTYCYCLE mode are from 1 to 7, with each integer increment in VCOTAP resulting in a 1/8 increment in duty cycle. The ispLEVER Module/IP Manager is recommended for generating the PLL module for DUTYCYCLE mode. In this mode, both MCLK and NCLK are in phase with the input clock CLKIN, thus reducing clock injection time. When in DUTYCYCLE mode, dividers DIV2 and DIV3 have no effect. Note: Non 50/50 duty cycle clocks will need to have manual constraints added to the preference file.

Example

If it is desired to have a clock with a duty cycle of 25% (25% high, 75% low), VCOTAP will be set to 2. The duty cycle is controlled by the following equation:

Clock high time = 1/8 * (VCOTAP)

PHSHIFT

In PHSHIFT mode, both MCLK and NCLK are active and may be used by the designer. The NCLK output is in phase with the input clock CLKIN, and the MCLK output is phase shifted with respect to the input clock. Therefore, MCLK lags NCLK by the value assigned to VCOTAP. The output clocks MCLK and NCLK are set to have a 50/50 duty cycle. When in PHSHIFT mode, dividers DIV2 and DIV3 have no effect. For external feedback, the NCLK output should be used to drive the feedback input to allow the MCLK output to be phase shifted (using the MCLK output to drive the feedback pin causes the NCLK output to be phase shifted backwards).

Example
To create an output clock from the PLL that is shifted 180 degrees with respect to the input clock, VCOTAP is set to 4. Valid values for VCOTAP are from 0 to 7 as indicated in Table 7. Each increment of VCOTAP value is associated with a 45 degree phase increment. The desired phase shift on the MCLK output is controlled by the following equation:

Phase shift = 1/8 clock cycle * VCOTAP value

DELAY

In DELAY mode, both MCLK and NCLK are active and may be used by the designer. The duty cycle of both MCLK and NCLK are set to 50/50 in DELAY mode, and the clocks can be delayed in the same way as in PHSHIFT mode using VCOTAP with the exception being that both MCLK and NCLK are delayed. However, if external feedback is used, both MCLK and NCLK will be aligned with the input clock, regardless of the value of VCOTAP. This mode is typically used with external feedback to remove the internal clock routing delays. The output MCLK and NCLK can be multiplied or divided according to the following equations:

Internal Feedback
Output frequency of MCLK = input frequency * DIV1/(DIV0 * DIV2)

Output frequency of NCLK = input frequency * DIV1/(DIV0 * DIV3)

External MCLK Feedback (MCLK Drives FB Pin)
Output frequency of MCLK = input frequency * DIV1/DIV0

Output frequency of NCLK = input frequency * (DIV1 * DIV2)/(DIV0 * DIV3)

External NCLK Feedback (NCLK Drives FB Pin)
Output frequency of MCLK = input frequency * (DIV1 * DIV3)/(DIV0 * DIV2)

Output frequency of NCLK = input frequency * DIV1/DIV0

Therefore, for internal feedback, the frequency can be multiplied up to 8x and divided up to 64x for both outputs. For external feedback, one clock frequency can be multiplied by up to 8x or divided up to 8x, but the other output can be multiplied or divided up to 64x. Only certain values are available between 8x and 64x. Only multiplication and division values that create PFD and VCO frequencies in the ranges shown in Table 4 are valid.

PLL_PHASE_BACK Preference Keyword
PLL_PHASE_BACK is a keyword that may be added to the preferences CLOCK_TO_OUT and INPUT_SETUP. Using this keyword in conjunction with CLOCK_TO_OUT and INPUT_SETUP reverses the offset direction of the phase delay programmed into the PLL. This will affect the reporting by TRACE, the timing utility included in the ispLEVER Project Navigator.

For example, suppose a user programs the PLL element to delay the clock by 7/8 of a clock cycle by using the PLL in PHSHIFT mode. TRACE will automatically add 7/8 of a clock cycle to the clock insertion delay by TRACE without the use of the keyword PLL_PHASE_BACK. By adding this keyword, TRACE is redirected subtracting 1/8 of a clock cycle which is the desired effect. This reduces the CLOCK_TO_OUT and increases the INPUT_SETUP time.

Use of this keyword gives the user the ability to control the desired effect of the PLL phase delay to match the user's intention and to be correctly reported in the TRACE timing tool. Below are examples of the syntax for the use of keyword PLL_PHASE_BACK. The user should be aware of the start-up one-cycle latency incurred by using this preference keyword and adjust the system accordingly.

```
CLOCK_TO_OUT_PORT<port_name> | GROUP <group_name> | ALLPORTS[<path_opt>] <time_spec>
[CLKNET [=] <clk_netname>] | [CLKPORT [=] <clk_portname>] [PLL_PHASE_BACK];

INPUT_SETUP_PORT <port_name> | GROUP <group_name> | ALLPORTS <timespec> [CLKNET] [=]
<clk_netname>] | [CLKPORT [=] <clk_portname>] [PLL_PHASE_BACK];
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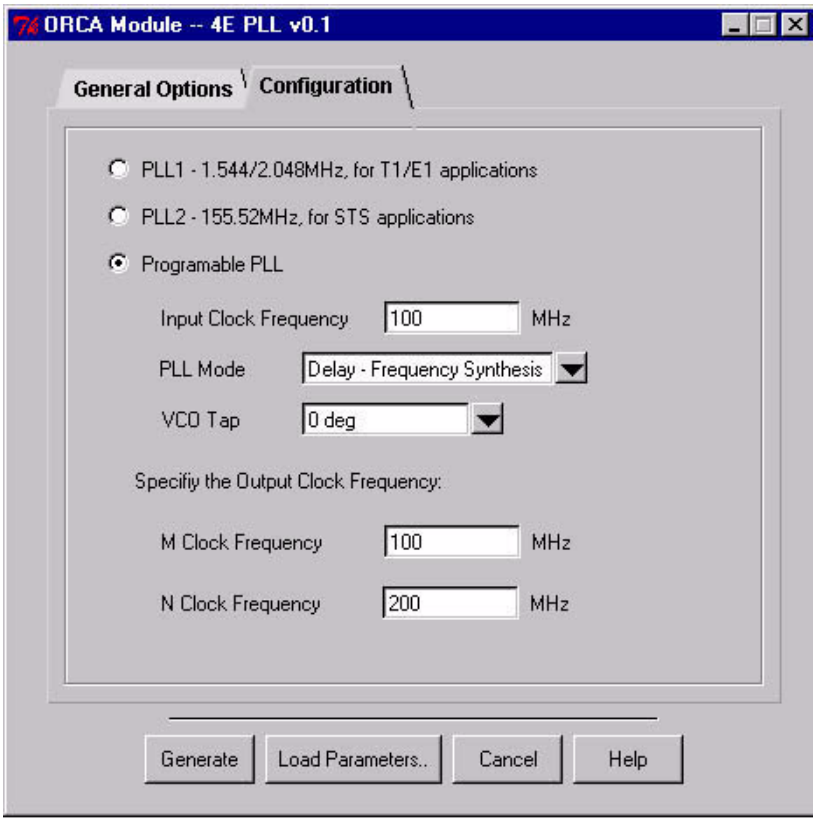
ispLEVER Module/IP Manager Usage for PLL Element Generation

The ispLEVER Module/IP Manager is a software HDL macro generator included with the installation of the ispLEVER Project Navigator. The ispLEVER Module/IP Manager supports generation of all four types of PLLs: PLL1, PLL2, PPLL, and HPPLL for the *ORCA* 4E family of FPGAs. The ispLEVER Module/IP Manager automatically calculates the appropriate attributes for the selected PLL based on options selected in the ispLEVER Module/IP Manager GUI.

Note: Selecting the appropriate synthesis vendor must be considered for the destination of the netlist, as each synthesis vendor treats attributes differently. Simulation attributes differ from synthesis attributes. One of the available selections for netlist destination is simulation. This destination should be selected when simulating with Model Technologies *ModelSim*®, and will generate the appropriate attributes for MTI simulation.

Figure 8 is a sample screen depiction of the ispLEVER Module/IP Manager GUI.

Figure 8. ispLEVER Module/IP Manager GUI



If the output frequency of any clock is found to be greater than 200 MHz, ispLEVER Module/IP Manager uses a HPPLL component. The ispLEVER Module/IP Manager reports a warning if the feedback frequency is greater than 420 MHz. Below is a description of the fields that display in ispLEVER Module/IP Manager for generating PLL HDL code.

PLL1, PLL2, Programmable PLL
Select from one of three options: PLL1, PLL2, or PPLL. An HPPLL component will automatically be generated when an output clock (MCLK or NCLK) is greater than 200 MHz.

Input Clock Frequency
Specifies the input clock frequency. This is a required parameter, and ispLEVER Module/IP Manager will prompt you to enter a value into this text box if none is given.

PLL Mode
Specify the mode of operation of the PLL. In the bypass mode, the output frequency is same as the input frequency. Both the output clocks have the same mode of operation.

VCO Tap
Specifies the VCO Tap. This is not available in the bypass mode. In DUTYCYCLE mode, it is used to control the duty cycle and while in PHSHIFT or DELAY mode it is used to phase shift the output clocks. A VCO Tap equal to zero is not allowed in DUTYCYCLE mode.

Specify the Output Clock Frequency
If M clock frequency is selected, the M clock output will be automatically computed. If N clock frequency is selected, the N clock output will be automatically computed. Both M clock and N clock frequencies may be specified. This option is available only in delay frequency synthesis mode.

Upon completion of entering the appropriate information in each field, press next, and the PLL HDL code will be generated and saved in the path selected.

Design Example

Figure 9, Figure 10, and Figure 11 are example test circuits used to illustrate how to minimize CLOCK_TO_OUT and INPUT_SETUP times using *ORCA* Series 4 PLL elements and their associated attributes. A PPLL component was used in the example and the input clock to the PLL was 100 MHz. No frequency multiplication/division or phase shifting was performed in this example.

Example #1: Minimizing CLOCK_TO_OUT and INPUT_SETUP Times

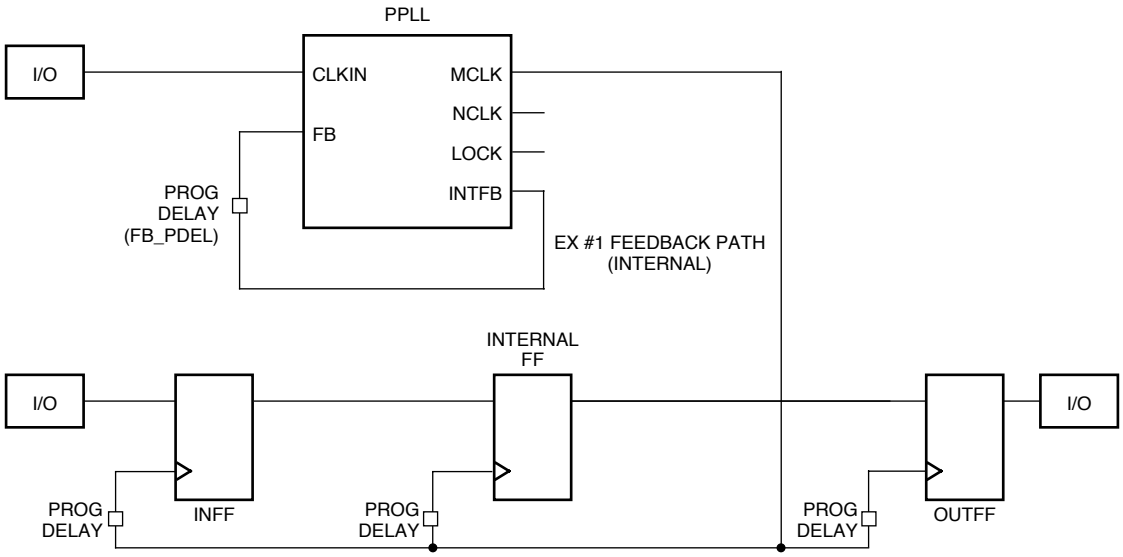
In example #1, the feedback used for the PLL was the INTFB output of the PLL. Using INTFB as the FB input will null out the delay of the PLL, but not the clock input buffer and clock routing. The attribute FB_PDEL cannot be used with INTFB as the FB input. From this, there are values of 9.538 ns and –4.253 ns for CLOCK_TO_OUT and INPUT_SETUP, respectively. INPUT_SETUP can essentially be considered to be zero, but a large hold time is incurred. This feedback path is generally not used in this way, but is instead intended to allow sophisticated control of the PLL feedback path using normal FPGA gates. All timing numbers were reported by TRACE.

Table 8. CLOCK_TO_OUT and INPUT_SETUP Example #1

FB Input	Add. Delay	INFF DEL	FB_PDEL	MCLK Frequency	CLK_TO_OUT	IN_SETUP
INTFB	NONE	DEL0	NONE	100 MHz	9.538 ns	– 4.253 ns

Note: CLK_TO_OUT and IN_SETUP are approximated.

Figure 9. Test Circuit for PLL Design Example #1



Example #2: Minimizing CLOCK_TO_OUT and INPUT_SETUP Times

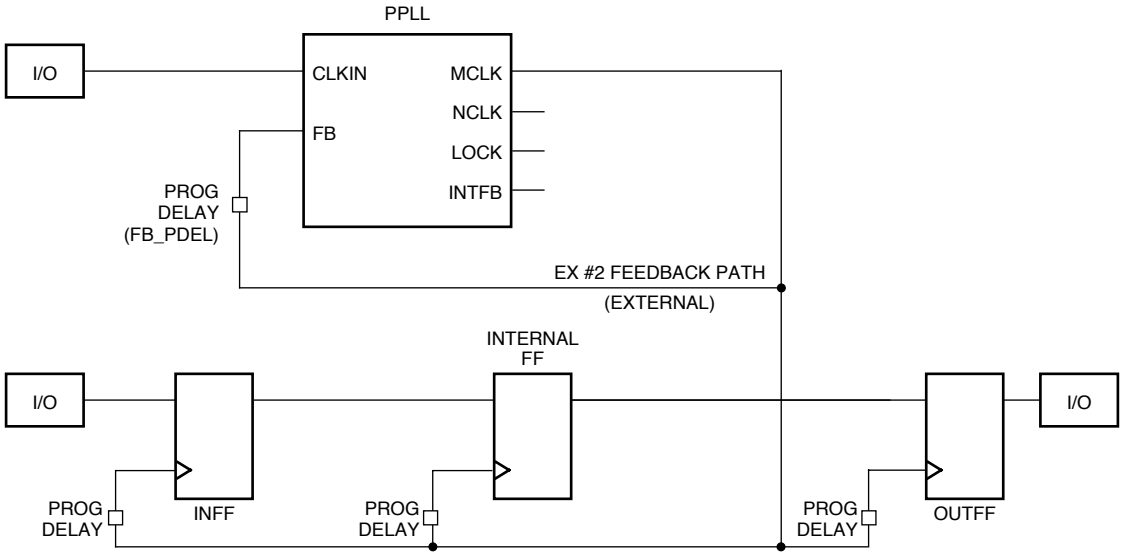
MCLK is now used as the FB input, see Figure 10. Using MCLK as the FB input nulls out the PLL delay as well as the routing delay of MCLK. From this, we can see a substantial reduction of CLOCK_TO_OUT from 9.538 ns to 1.341 ns, resulting in an 8.197 ns improvement. However, as a trade-off, INPUT_SETUP increased from 0 ns to 3.955 ns.

Table 9. CLOCK_TO_OUT and INPUT_SETUP Example #2

FB Input	Add. Delay	INFF DEL	FB_PDEL	MCLK Frequency	CLK_TO_OUT	IN_SETUP
MCLK	YES	DEL0	DEL0	100 MHz	1.341 ns	3.955 ns

Note: CLK_TO_OUT and IN_SETUP are approximated.

Figure 10. **Test Circuit for PLL Design Example #2**



Example #3: Minimizing CLOCK_TO_OUT and INPUT_SETUP Times

Example #3 uses the same configuration as example #2, but with the addition of programmable delay to the clock of the I/O FF, INFF. This improves INPUT_SETUP iby the value associated with the DEL3 attribute of the I/O FF (2 ns). The programmable delay values (DEL0, DEL2 and DEL3) associated with the I/O FFs are the same as those used for the programmable FB_PDEL in example #2.. This INFF delay element is a unique feature on ORCA FPGAs. This advanced design technique is available with the ASIC preference. For this example, the following preference can be used to set the FB_PDEL to a DEL3 value:

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ASIC "my_pll" TYPE "PPLL" FB_PDEL=DEL3;
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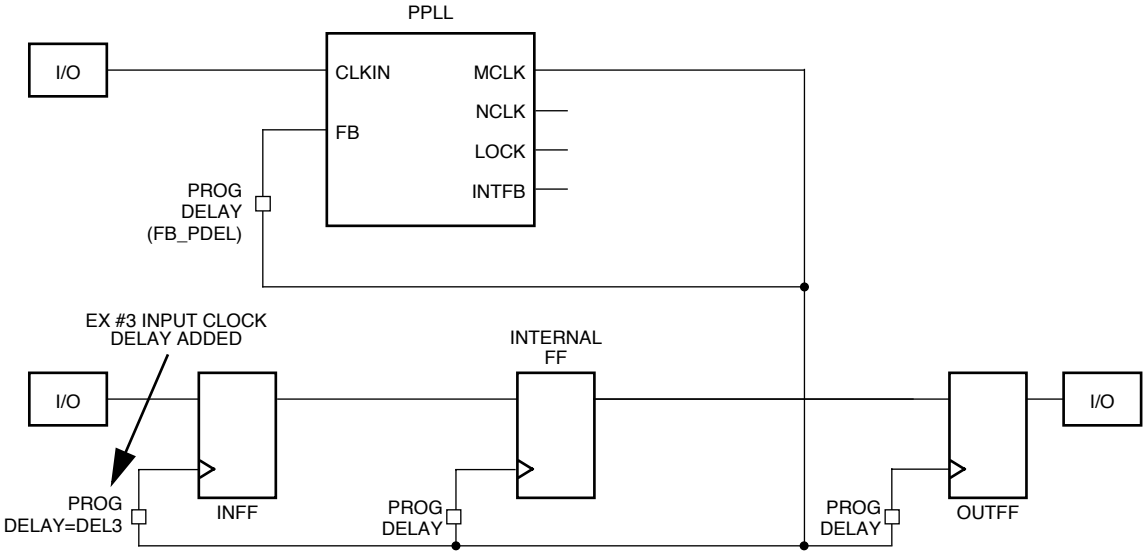
Table 10. CLOCK_TO_OUT and INPUT_SETUP Example #3

FB Input	Add. Delay	INFF DEL	FB_PDEL	MCLK Frequency	CLK_TO_OUT	IN_SETUP
MCLK	YES	DEL3	DEL0	100 MHz	1.341 ns	1.976 ns

Note: CLK_TO_OUT and IN_SETUP are approximated.

Figure 11. Test Circuit for PLL Design Example #3



In conclusion, to minimize CLOCK_TO_OUT delay in an ORCA Series 4 FPGA, designers should use either MCLK or NCLK as the FB input depending which is used, and add the appropriate programmable feedback delay to the feedback path using the FB_PDEL attribute. To decrease the INPUT_SETUP, the input FF delay element should be included with the appropriate delay specified. Other combinations also use the phase delay capabilities of the PLLs, together with the FB_PDEL, INFF, and OUTFF programmable delays. Source code for these three examples can be found at the Lattice Semiconductor Inc. website, http://latticesemi.com.

Lock Signal

The LOCK output signal from each PLL is used to determine when a given PLL is locked to the input clock. This signal needs to be integrated over time so that it does not pulse high during lock acquisition and so that glitches do not occur during normal operation. Any glitch of duration greater than or equal to one clock cycle should be considered an out of lock condition.

This signal can be used to verify that the PLL remains locked. Another application that the LOCK pins can be used for is to delay the end of configuration of the FPGA or FPSC until a PLL has locked. The LOCK signal of multiple PLLs can be ANDed and sent to the FPGA/FPSC STARTUP block for this purpose. The Series 4 data sheet has more information on how to use the STARTUP block to delay the end of configuration.

General PLL Design Considerations

- When phase shifting is used with the PPLL or HPPLL elements, it is very important that the feedback path to the FB input pin be chosen carefully. If internal feedback is used, connecting the INTFB output to the FB input, then any amount of phase shifting can be done on the MCLK output. If external feedback is used, then the NCLK output must be chosen to perform the feedback (in PHSHIFT mode NCLK is unshifted while MCLK is shifted. Using the phase shifted MCLK as external feedback would result in no phase shift at all.)
- The PFD operating frequency (see Figure 4) must always stay within its operating range. For PPLL, the valid range is 2.0 MHz to 200 MHz. For HPPLL, the valid range is 7.5 MHz to 420 MHz. The PFD operating frequency is always equal to CLKIN/DIV0.When calculating multiplication and division values for the PPLL and HPPLL elements, the VCO operating frequency (see Figure 4), must always stay within their operating range. For PPLL the valid range is 15 MHz to 200 MHz, while HPPLL has a valid range of 60 MHz to 420 MHz. When ispLEVER Module/IP Manager is used to generate the needed PLLs it will ensure that the VCO stays within its operating range. For example, if internal feedback is chosen, MCLK=Input Frequency*DIV1/(DIV0*DIV2), and NCLK=Input Frequency*DIV1/(DIV0*DIV3) must be within this operating range.
- In the PPLL and HPPLL elements, the feedback (FB) input can be driven by any periodic signal based on the MCLK or NCLK outputs from the PLL. This includes the allowance for the feedback signal to be a version of the MCLK or NCLK outputs that had been driven off-chip and then brought back onto the chip and into the FB input. The requirement is that this signal path must be able to pass clock pulses that are 20% shorter than the minimum pulse for the PLLs times either the value of DIV2 if MCLK is used for feedback or DIV3 if NCLK is used for feedback (the clock phase that must be passed for PPLL = 4.2 ns period, HPPLL = 2.0 ns period).
- By default, all clock outputs from a PLL (NCLK and MCLK) use primary clock routing resources. If desired, outputs can be forced onto secondary clock routing resources with the use of the USE SECONDARY preference, in the preference file. See the ispLEVER help system for preference file syntax.
- If dedicated PLL clock pins are not initially selected for a design and a PLL needs to be added later, it is possible to add the PLL without using the dedicated PLL clock pins. However, It is good design practice to include additional traces connecting non-PLL clocks to PLL dedicated inputs in case they are needed after PCB fabrication. The consequence of not using the dedicated PLL clock pins is added clock insertion delay to the design. Note that the dedicated pins must always be used for the PLL1 and PLL2.
- PLLs may drive an internally generated clock. This is accomplished by attaching (wiring) the clock net to an output pin of the PLL. The programmable PLLs can also be driven by internally generated clocks.
- All programmable PLL parameters in Series 4 FPGAs and FPSCs can be modified without requiring re-configuration by accessing the registers that control the PLLs through the system bus. This allows designers to try different PLL configurations such as clock phase and duty cycle quickly on the board. More information is available in the ORCA Series 4 MPI/System Bus Technical Note (TN1017).
- FB_PDEL is an attribute that can be used to null out clock delay to achieve fast clock-to-out delays in I/O FFs. Using FB_PDEL with a corresponding value from DEL0 to DEL3 adds delay to the feedback path which in turn decreases clock insertion delay and clock-to-out. The values of DEL0, DEL1, DEL2, and DEL3 are shown in Table 6. For example, DEL1 corresponds to 0.5 ns delay.
- FB_PDEL has no effect unless the FB input is driven by an external signal, since the delay is inserted in the incoming routing. In particular, FB_PDEL has no effect when the FB input is driven by the INTFB output of the same PLL.
- When a clock signal used as feedback to the PLL is a different frequency than the input clock frequency, the PLL design cannot guarantee a consistent phase relationship between the feedback signal and the input clock.