Using Power/Platform Management Device HVOUTs to Drive MOSFETs

November 2011 Application Note AN6043

Introduction

Power/Platform Management devices are a complete single-chip solution for monitoring and sequencing power supplies for circuit boards and systems with multiple voltages. Programmable logic based equations and sequence controller forms the functional core of a Power/Platform Management device along with programmable timers. The outputs of the programmable logic control the Power/Platform Management device outputs directly.

These devices have high-voltage MOSFET drivers with both programmable output currents and voltage limits. By controlling gate charging currents, and consequently gate voltage slew rates, Power/Platform Management devices can be used to provide a soft-start function for MOSFET power switches. This application note describes the operation and use of the Power/Platform Management device MOSFET driver outputs.

See Tables 1 and 2 for the Power/Platform Management devices applicable to this application note.

Table 1. Applicable Power Manager Devices Summary

Device	VMONs	Digital Inputs	HVOUTs	Open Drain Outputs	Trim DAC Outputs	CPLD Macrocells
ispPAC®-POWR607	6	2	2	5	None	16
ispPAC-POWR1014/A	10	4	2	12	None	24
ispPAC-POWR1220AT8	12	6	4	16	8	48

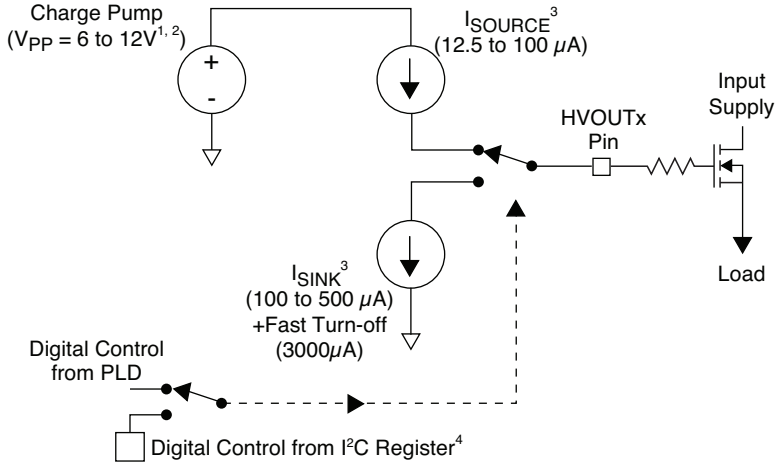
Table 2. Applicable Platform Manager™ Devices Summary

Device	VMONs	Digital Inputs	HVOUTs	Open Drain Outputs	Trim DAC Outputs	Digital I/O	CPLD Macrocells	FPGA LUTs
LPTM10-1247	12	4	4	12	6	31	48	640
LPTM10-12107	12	4	4	12	8	91	48	640

MOSFET Driver Operation

Figure 1 shows the details of the HVOUT gate drivers. Each of these outputs may be controlled from the programmable logic or I²C registers (except for the POWR607 and POWR1014 non-'A' devices).

Figure 1. Basic Function Diagram for an Output in High Voltage MOSFET Gate Driver Mode

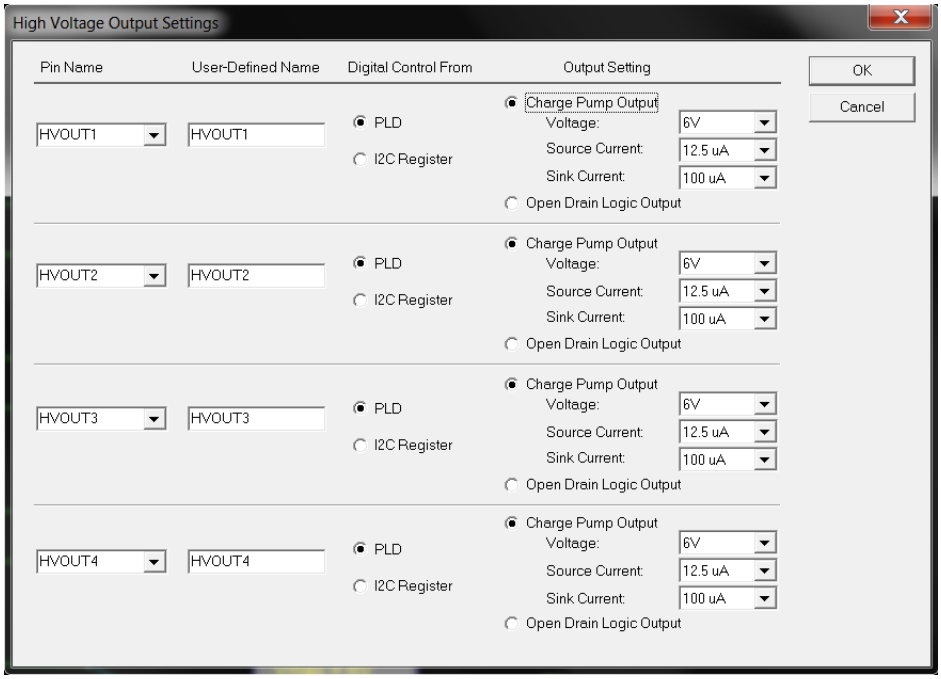


1. For POWR1014/A, -01 performance grade devices provide three selectable output voltage settings from 6V to 10V in 2V steps. The -02 performance grade devices also support the 12V output voltage setting.
2. For POWR607, only the 9V fixed charge pump output is available on HVOUT pins.
3. For POWR607, I_{SOURCE} is fixed at 15uA and I_{SINK} is typically 2.5mA (1mA min.).
4. Digital control from I^2C registers is not available in POWR607 and POWR1014 non-'A' devices.

A LOW output from the sequence controller/I^2C register will cause the switch to connect the output to I_{SINK} and the driver will attempt to sink current from the load attached to ground. When a HIGH signal from the sequence controller/I^2C register sets the switch to its other position, the output is connected to I_{SOURCE} and the driver will attempt to source current into whatever load is attached to its output pin. In this latter case, the maximum voltage to which the current source can drive a load is limited to VPP by circuitry inside the driver based on the Power/Platform Management device chosen, represented here by a voltage source. Although the devices are designed to operate typically at 3.3V, internal charge-pump circuitry provides the I_{SOURCE} current source with the ability to drive the output pin as high as 12V.

The HVOUT driver circuits available in each device can be individually configured. Both I_{SOURCE}, I_{SINK} and VPP can be independently programmed for each of the outputs. PAC-Designer® software provides a dialog box, shown in Figure 2 for this purpose (view changes with available options). Each driver output may be configured in one of two modes, charge-pump output mode or open-drain logic output mode. For driving MOSFETs, the driver should be configured for charge-pump mode. Output control can be chosen as either programmable logic or I^2C register.

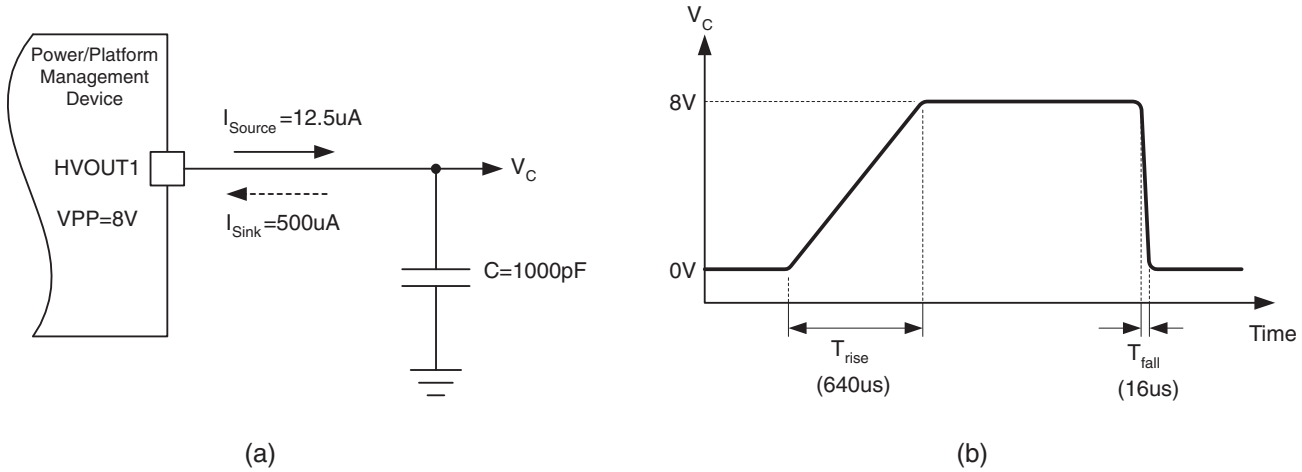
Figure 2. High-Voltage Output Settings Dialog for POWR1220AT8



When a driver is set to charge-pump mode, drop-down list boxes are enabled to specify the maximum voltage to which the output can drive the load (VPP), source current (I_{SOURCE}) and the sink current (I_{SINK}).

When this source current is fed into a capacitive load (Figure 3a), the output voltage rises in time as a linear ramp (Figure 3b). The voltage will continue rising either until the current source is turned off or the output voltage reaches the current source's compliance limit (VPP). In the case shown here, the output voltage has been limited by the Power/Platform Management device's VPP limit, here set to 8V. *Note: For POWR607, these settings are not possible. Only a VPP of 9V, source current of 15uA and a minimum sink current of 1mA are available.*

Figure 3. Controlled Rise and Fall Times of Capacitive Load



For a given value of charging current and a given value of load capacitance, the rate-of-change in voltage across the load capacitor is given by:

$$\frac{dV}{dT} = \frac{I}{C} \quad (1)$$

For the example shown in Figure 3, a 10µA charging current into a 1000pF capacitor yields a voltage slew rate of $12.5x10^{-6}$ A /$1000x10^{-12}$ F = 12,500 V/s. This results in a rise time of 640µs to go from 0V to 8V.

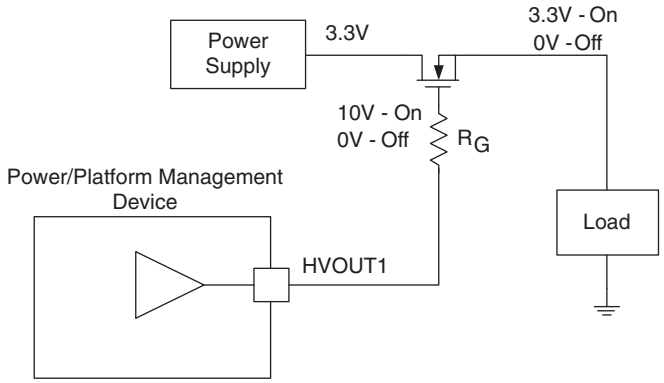
Conversely, when the Power/Platform Management device's output sinks current, the voltage across the load capacitor will ramp down. Because the sink current is much greater (500µA) than the source current, the load capacitor voltage will ramp down (500,000 V/s) much faster to zero volts than it ramped up.

Because the gate of a MOSFET appears as a capacitor to the circuitry driving it, a constant-current gate driver can be used to turn on a MOSFET at a controlled rate. In a typical power distribution system many of the loads to be controlled may have a significant capacitive component. Engaging these loads to the main supply over the course of few hundred microseconds or a few milliseconds can prevent the load capacitance from pulling excessive current from the main supply and causing it to momentarily dip.

While charge-pump circuitry on the Power/Platform Management device enables the I_{SOURCE} current source to charge a load considerably beyond the device's VDD supply rail (as high as 12V with a 3.3V VDD), allowing the output to climb to this maximum voltage is not always desirable. Many contemporary low-voltage power MOSFETs have thin gate oxides and correspondingly low maximum gate-to-source voltage (V_{GSmax}) ratings (<12V). For this reason, the Power/Platform Management device supports independently programmable voltage limits on each MOSFET driver output. These limits may be set from 6V to 12V, in increments of 2V. The maximum permissible output voltage for the MOSFET drivers is also dependent upon the Power/Platform Management device used. For POWR607, charge pump output is fixed at 9V.

The utility of a high-voltage output drive capability becomes apparent when looking at Figure 4. In this circuit, an N-channel MOSFET is used to switch power to the load. N-channel MOSFETs are preferred in many power electronic applications because they tend to have lower on-resistances and higher voltage ratings than P-channel devices of similar form-factors and costs. In a high-side application, such as the one shown here, it is necessary to drive the gate to a voltage (V_G) significantly higher than that of the source (V_S) to completely turn the device on. In this particular example, a gate-source voltage (V_{GS}) of 6.5V is needed to fully activate the device. Because the MOSFET's source will be at 3.3V when the circuit is fully on, at least 9.8V will be need to be applied to the gate terminal. By providing an on-chip high-voltage source, the Power/Platform Management device's internal charge pumps greatly simplify design when N-channel MOSFETs are to be used in high side switching applications.

Figure 4. Driving N-Channel MOSFET with Power/Platform Management Device Output



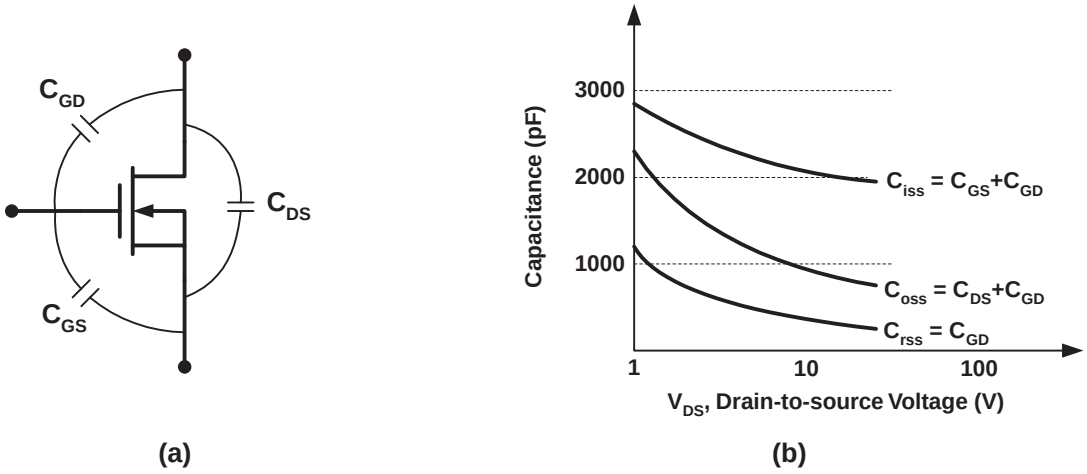
To reduce the possibility of RF oscillation, a gate resistor (R_G) is often inserted in series with the gate of the MOSFET power switch. This resistor should be placed physically close to the MOSFET gate terminal, and connected by as short a PCB trace as is feasible. An appropriate value for these gate resistors is highly dependent on both the characteristics of the MOSFET being used and the circumstances of the application, but will often be in the range of 10 to 100 ohms.

Predicting MOSFET Turn-on Time

Because the Power/Platform Management device's MOSFET output drivers source a precise and well-defined output current, it becomes possible to predict MOSFET gate rise times if one knows the value of the load capacitance presented by the MOSFET being driven.

Although a MOSFET is a capacitive load, the effective value of this capacitance can be quite complicated to estimate. This is because there are actually several different sources of capacitance in a MOSFET, as shown in Figure 5a. The total capacitance seen at the gate terminal by a driver will also be highly dependent on the details of the circuit the MOSFET is part of, and how it functions in that circuit.

Figure 5. Model of MOSFET Internal Capacitors

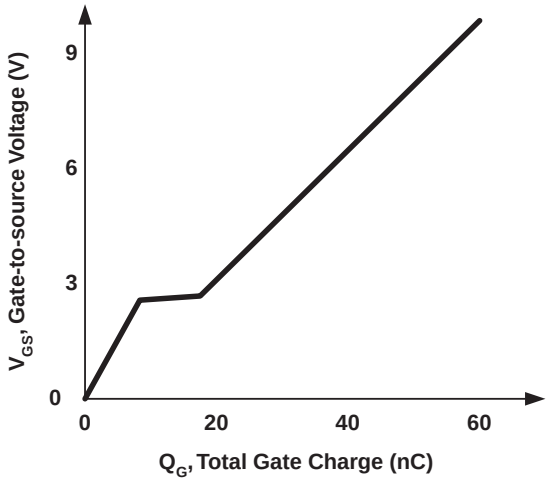


Additionally, each of the MOSFET's capacitors may vary as a function of bias voltage, drain current, and temperature. Figure 5b shows an example of how a typical MOSFET's capacitances vary as a function of drain-to-source voltage (V_{DS}). This type of characterization data is most useful in situations where bias is nearly constant, such as in linear amplifier circuits.

Fortunately, there are methods for characterizing a MOSFET's effective gate capacitance when the device is used in switching applications. One such method is not by trying to define capacitance, but rather by defining the amount

of total charge that needs to be pumped into the MOSFET's gate in order to turn it on. Figure 6 shows an example of this type of characterization, in which VGS (Gate-to-Source Voltage) is plotted versus total gate charge.

Figure 6. MOSFET Gate Charge vs. Gate-Source Voltage



Using this model, it becomes straightforward to estimate the gate rise time for a given charging current. For the circuit of Figure 4, the MOSFET's source voltage (V_S) will be 3.3V when the device is fully switched on, while the gate voltage (V_G) will be 10V in this condition. The device's gate-to-source voltage (V_{GS}) will therefore be 6.7V. Reading across and down the plot of Figure 6, a V_{GS} of 6.7V corresponds to ~40 nC of gate charge (QG). Because charge is equal to the product of current (I) and time (T_{charge}) when current is constant, gate charging time can be expressed as:

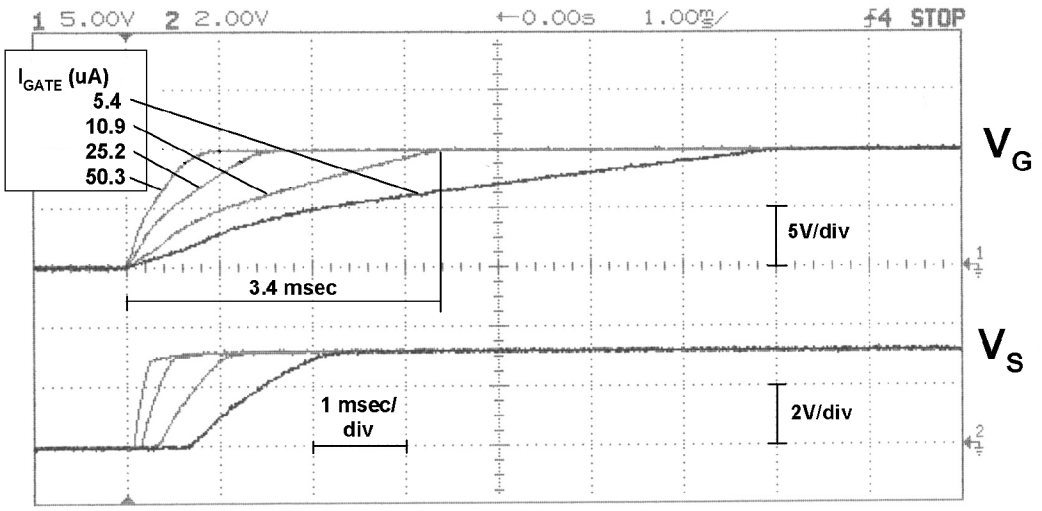
$$T_{charge} = \frac{Q_G}{I} \quad (2)$$

For this example, let us assume a charging current of 12.5µA. Gate charging time is given by:

$$T_{charge} = \frac{40 \times 10^{-9} C}{12.5 \times 10^{-6} A} = 3.2 \times 10^{-3} \text{ s} \quad (3)$$

Validation of this result can be seen in Figure 7. The top set of traces shows gate rise times for various (5.4µA to 50.3µA) gate drive currents. The trace labeled 10.9µA shows a 0-10V rise time of 3.4 milliseconds, which agrees to within 10% of our predicted value, well within the limits of device-to-device variation.

Figure 7. Gate and Source Voltage Responses for Circuit of Figure 4



Although predicting the response of the gate is straightforward, estimating the rate at which the load will turn on is considerably more difficult. The lower set of waveforms in Figure 7 shows the rise of the MOSFET source voltage, indicating the actual turn-on rate of the load. When the gate voltage crosses the MOSFET's threshold voltage, the MOSFET begins to conduct. This appears as a delay between the time at which the gate voltage begins ramping and when the source voltage begins to rise. Note, however, that in the case above, the MOSFET moves into a completely 'ON' condition well before the gate voltage reaches its maximum limit. For any given MOSFET, the time required to achieve an 'ON' state will be dependent on both the steady-state current consumption of the load and the amount of load capacitance which needs to be charged.

Because the Power/Platform Management device provides programmable output carried over a wide range, a system designer can tune the actual MOSFET turn-on times by merely programming the appropriate current values. In-system programmable $E^2CMOS^{®}$ technology supports over 1,000 programming cycles per device, making an iterative approach feasible. In cases where tight control of turn-on times need to be maintained, devices can also be trimmed on a unit-by-unit basis. In-system programmability also lends itself to the implementation of cost-effective automated test-and-trim systems for high-volume manufacturing environments.

PAC-Designer provides the simulation tool "Power Manager_HVOUT_Sim.exe" as one of the design utilities. For more information, see AN6070, Using the HVOUT Simulator Utility to Estimate FET Ramp Times.

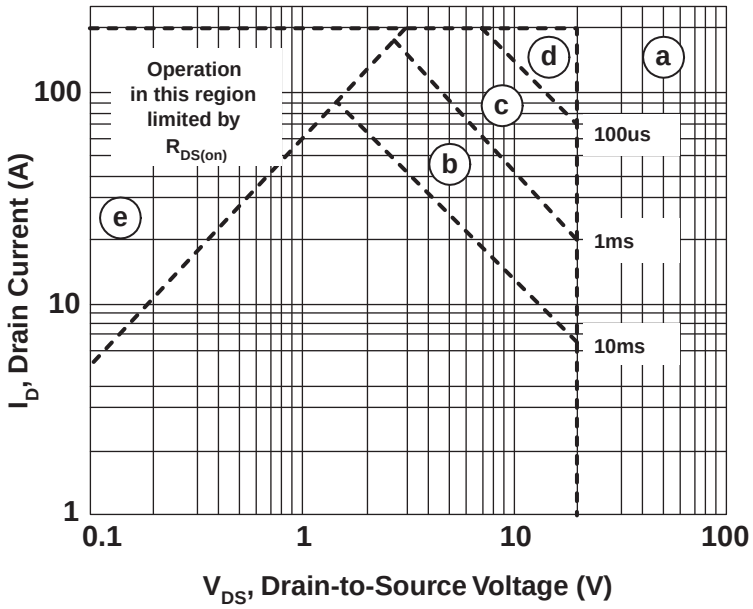
Additional Topics

In addition to the issue of how fast the MOSFET can be turned on and off, there are several other issues that are associated with successfully implementing a high-side power switch when using the Power/Platform Management device and discrete MOSFETs. The following sections describe a few of the more significant ones.

Safe Operating Area

It is possible to obtain surface mount MOSFETs that can handle tens of Amperes of drain current and hundreds of Volts of drain-to-source voltage. The caveat is that while these devices can handle both high voltages and currents, they can't handle them both at the same time, at least not for very long. For this reason, power MOSFETs are characterized with a set of Safe Operating Area (SOA) curves, an example of which is shown in Figure 8.

Figure 8. Safe Operating Area (SOA) Curves



SOA curves are significant in the design of 'soft-start' power switches in that the power MOSFETs used to implement these switches may remain in their linear operating regions for significant amounts of time (milliseconds). Ordinarily, power switches are operated either completely on, with high I_D and near-zero $V_{DS,}$ or completely off, with zero I_D and high $V_{DS.}$ In either of these cases, the device's power dissipation is relatively low ($P_D = I_D \times V_{DS}$). Very little time is spent in transition between the MOSFET's ON and OFF states. In contrast, when a MOSFET is turned on slowly, the device may spend a significant amount of time (milliseconds) in a condition where both V_{DS} and I_D are non-zero, with a correspondingly high power dissipation.

SOA curves define a set of bias condition boundaries within which a device may be safely operated. Figure 8 shows an example of a set of SOA curves for a typical low-voltage power MOSFET. The various regions and boundaries have been denoted (a) - (e). Region (a), which covers those areas of device operation in which I_D > 200A or V_{DS} > 20V defines a set of operating conditions which may immediately damage the device, regardless of how short an interval the device operates under these conditions.

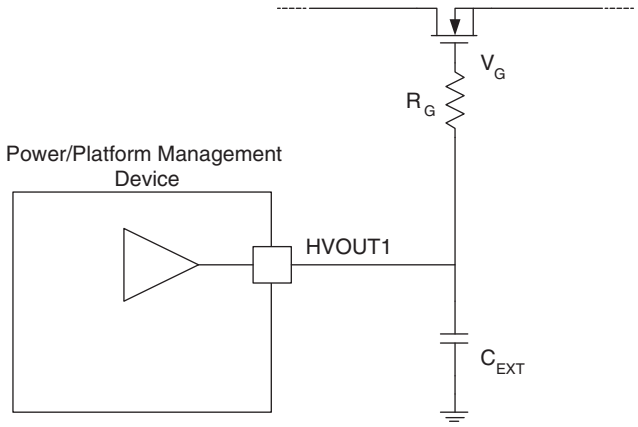
The curves labeled (b) through (d) define conditions under which the device may be safely operated for a limited amount of time. For example, the device may be operated for up to 100 microseconds anywhere below the (d) curve, up to 1 millisecond anywhere below the (e) curve, and up to 10 milliseconds anywhere below the (b) curve. Note that these operating times are specified for single-pulse operation; a series of consecutive pulses of these durations may still overstress the device.

Finally, region (e) defines a set of operating conditions under which the MOSFET cannot be made to operate. This is when V_{DS} is too low to force the specified amount of current (I_D) through the device regardless of how hard the gate is driven. The boundary of this region is of particular interest to the power-supply designer because it places a lower limit on V_{DS} drop that can be expected for a given amount of drain current.

Getting Long Turn-on Times Without Using Low Gate Current

If a long MOSFET turn-on time is needed, an alternative to using very low gate drive currents is to artificially increase the gate capacitance with an external capacitor. Figure 9 shows how this is done.

Figure 9. Slowing Down Turn-on Rate with Additional Capacitance



The external capacitor adds to the MOSFET's gate capacitance. The simplest way to estimate the new gate rise time to 'V' Volts is to add the total gate charge (from the chart in Figure 6) to the charge required to charge the external capacitor (Q=CEXTVG), and then calculate rise time from the total charge required to bring both the MOSFET gate and capacitor to the target voltage.

$$T_{charge} = \frac{Q_G + Q_{EXT}}{I} = \frac{(Q_G + Q_{EXT}V_G)}{I} \quad (4)$$

Note that because the external capacitor is referenced to ground, its charge derives from V_G as opposed to the case of the MOSFET, where the gate charge is derived from V_{GS}.

Summary

This application note has described the function of the Power/Platform Management device's MOSFET output drivers. These devices' variable current MOSFET driver outputs support soft-start switching capabilities which help to reduce power supply transients resulting from large, uncontrolled current surges. Power/Platform Management devices are ideally suited for controlling the high-side power MOSFET switches commonly used in modern on-board power management systems.

Related Literature

- DS1011, ispPAC-POWR607 Data Sheet
- DS1014, ispPAC-POWR1014/A Data Sheet
- DS1015, ispPAC-POWR1220AT8 Data Sheet
- DS1035, Platform Manager Data Sheet
- AN6070, Using the HVOUT Simulator Utility to Estimate FET Ramp Times

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Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
November 2011	01.2	Updated to cover a broader range of Power/Platform Management devices.