Using ispGDX™, ispLSI® 2000VE and 5000V Devices in "Hot-Swap" Environments

Introduction

This document describes the input and I/O characteristics of Lattice ispGDX, ispGDXV™, ispLSI 2000VE and 5000V devices for live plug-in, "hot-swap" applications.

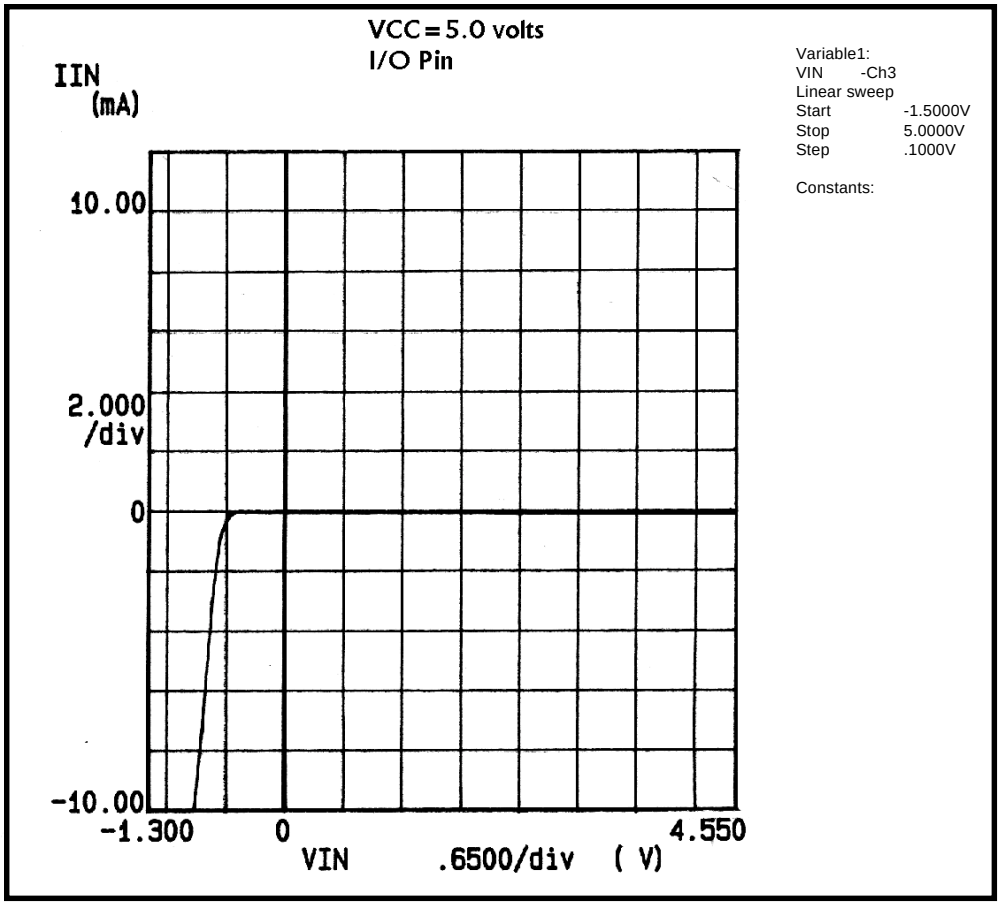
Lattice ispGDX, ispGDXV, ispLSI 2000VE and 5000V devices are used extensively in communications system boards that interface with the PCI, EISA, VME and proprietary bus configurations where hot-swapping is very common. When hot-swapping the boards for servicing, certain input and I/O characteristics are required to ensure proper operation of the system.

I/O Characteristics

The input and I/O voltage/current characteristics of the ispGDXV, ispLSI 2000VE and 5000V devices (V_{CC}=3.3V and V_{CC}=0.0V) and ispGDX160 device (V_{CC}=5.0V and V_{CC}=0V) illustrate how the parts will behave during power-up and power-down cycles. It is very important not to have abnormal current rises on the pins during hot-swapping of the boards and to know when the device outputs turn on/off during a power up/down cycle.

Figures 1-8 show the voltage vs. current for an input pin (or an I/O pin configured as input) for the ispGDX, ispGDXV, ispLSI 2000VE and 5000V respectively. These graphs show both conditions V_{CC}=3.3V (V_{CC}=5.0V for ispGDX160) and V_{CC}=0V. The input voltage is swept from -1.5V to +5.0V for the ispGDX160, from -0.7V to 5.0V for the ispGDXV, from -1.3V to 5.2V for the ispLSI 2000VE and from -1.8V to 3.6V for the ispLSI 5000V. The plots do not show any current surges in the positive voltage range as long as the input voltage condition is within the TTL logic level. The current starts to increase as the voltage is swept in the negative direction as a result of the input clamp (ESD) protection circuitry.

Figure 1. ispGDX Input and I/O Characteristic With V_{CC} Applied



Figures 9, 11, 13 and 15 illustrate the V_{CC} level at which an output pin becomes active. In this case, output is registered. The V_{CC} level at which ispGDXV, ispLSI 2000VE and 5000V start to switch is approximately 1.5V to 2.0V. The value of V_{CC} at which ispGDX starts to switch is 3.0V. Figures 10, 12, 14 and 16 illustrate the power-off condition where the outputs stop to switch. It is approximately 1.0V to 1.5V. The absolute maximum V_{CC} specification of 5.4V for the ispGDXV, ispLSI 2000VE and 5000V and 7.0V for the ispGDX160 must be satisfied all times.

It is recommended to tie off the JTAG pins high if a board is to be used in a "hot-swap" environment. This can be accomplished by setting TMS, TDI and TCK pins high using a resistor in the range from 4.7K to 10K Ohm.

Summary

In summary, the ispGDXV, ispGDX, ispLSI 2000VE and 5000V device I/Os show no input current discontinuity during power-up and power-down. This characteristic, combined with the control of the external signal sources driving the I/O pins to TTL logic voltage levels, will prevent the device from going into undesirable states.

Technical Support Assistance

Hotline: 1-800-LATTICE (Domestic)
1-408-826-6002 (International)

e-mail: techsupport@latticesemi.com

Figure 2. ispGDX Input and I/O Characteristic Without V_{CC}

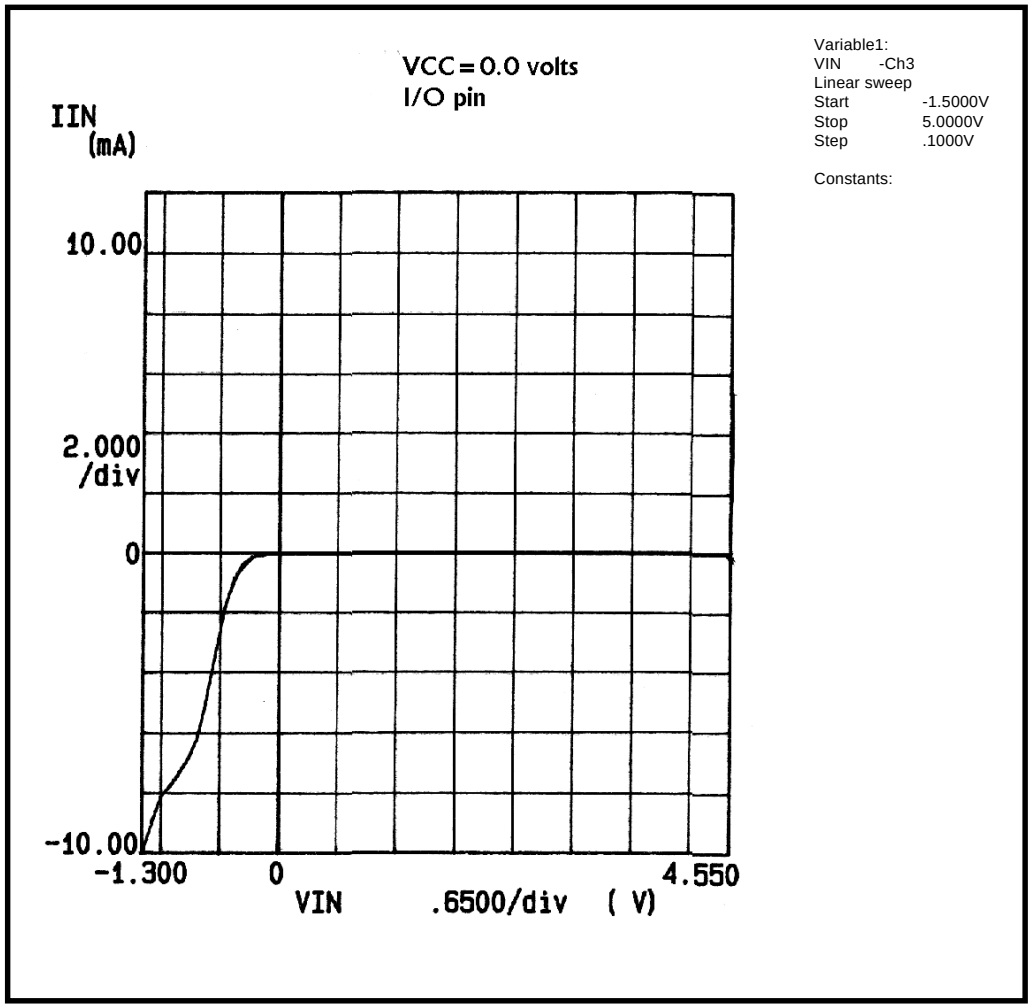


Figure 3. ispGDXV Input and I/O Characteristic With V_{CC} Applied

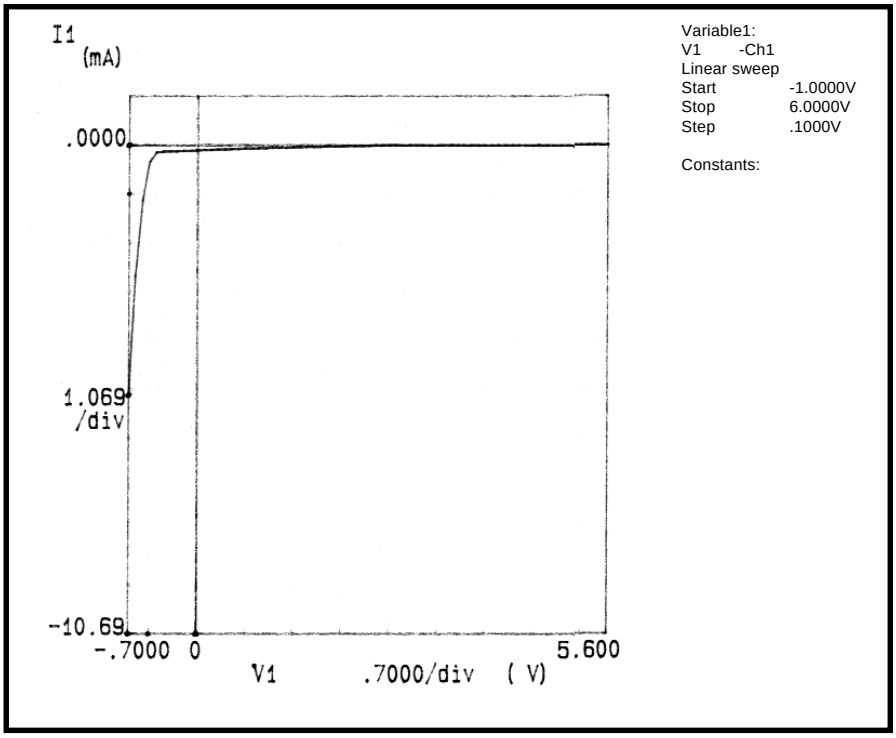


Figure 4. ispGDXV Input and I/O Characteristic Without V_{CC}

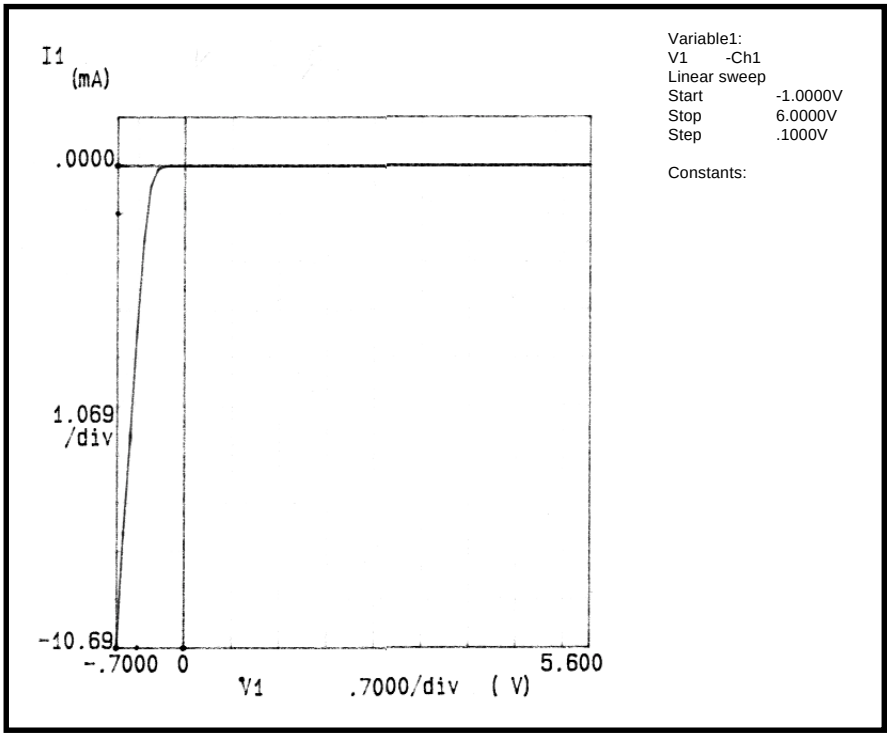


Figure 5. ispLSI 2000VE Input and I/O Characteristic With V_{CC} Applied

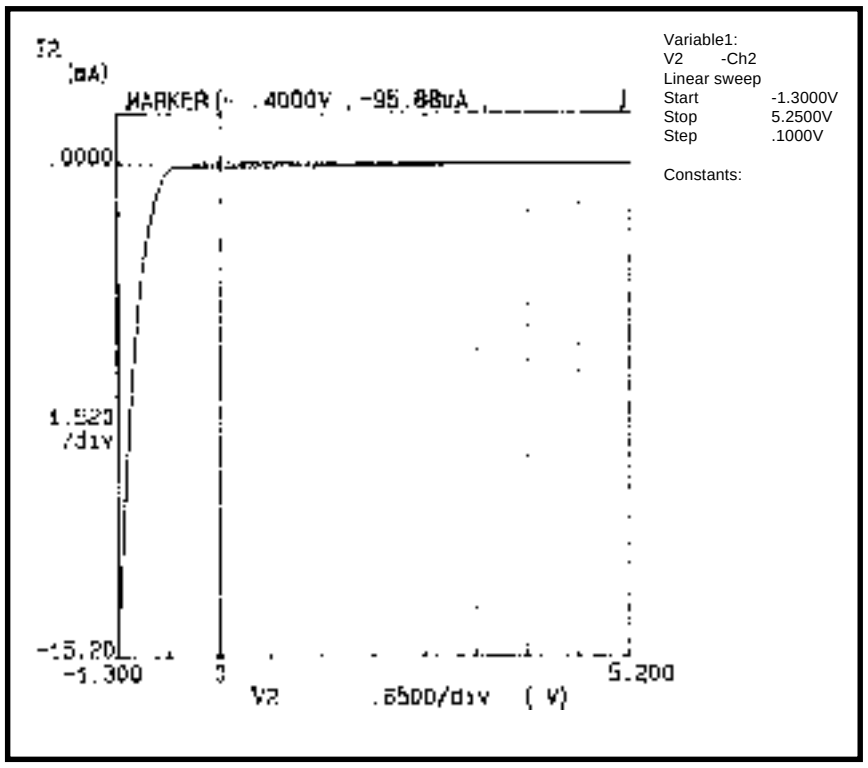


Figure 6. ispLSI 2000VE Input and I/O Characteristic Without V_{CC}

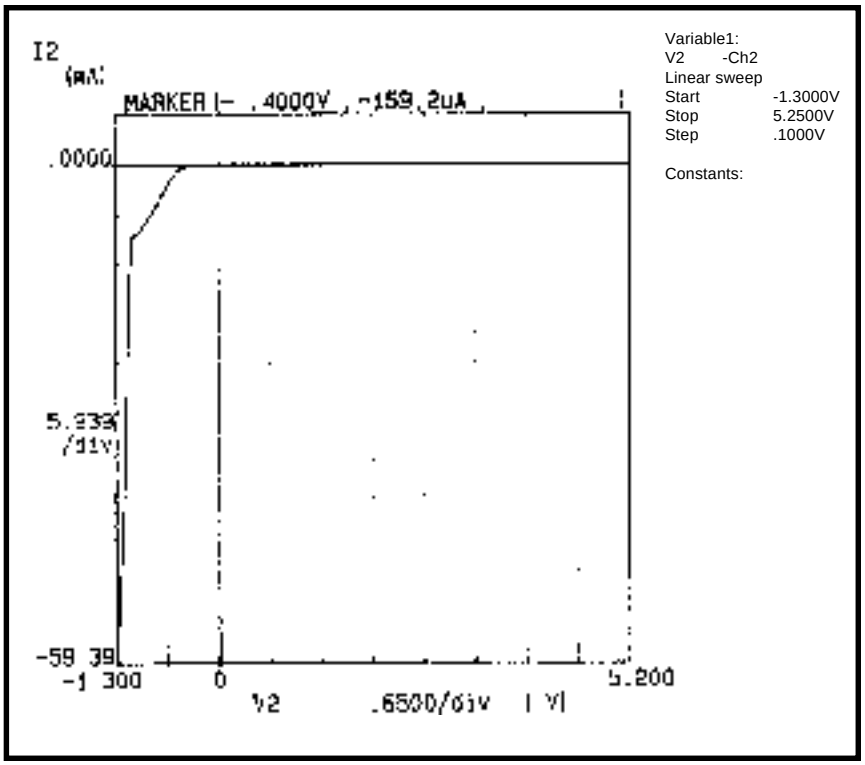


Figure 7. ispLSI 5000V Input and I/O Characteristic With V_{CC} Applied

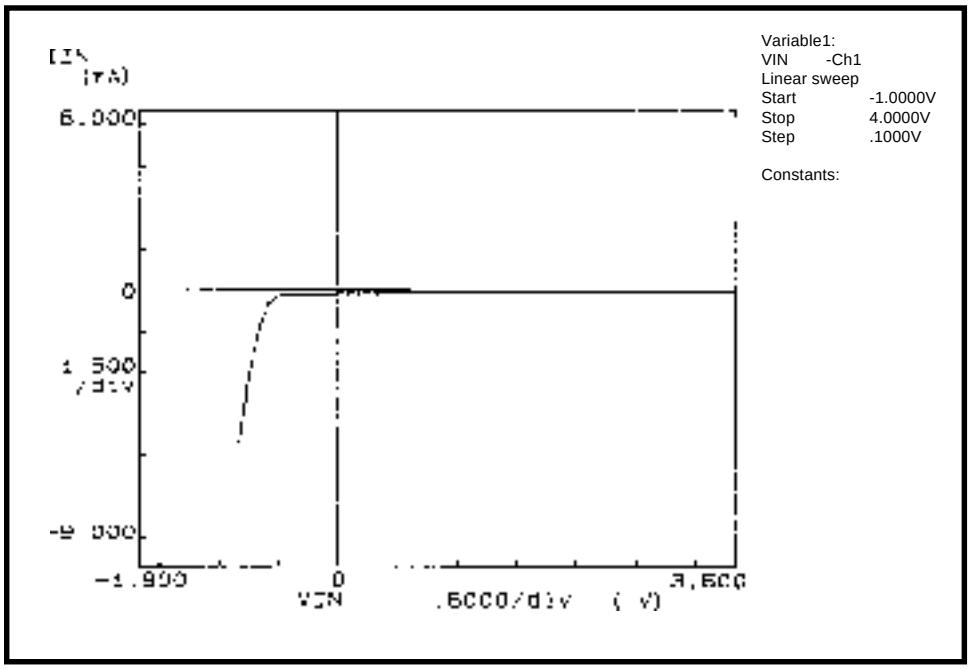


Figure 8. ispLSI 5000V Input and I/O Characteristic Without V_{CC}

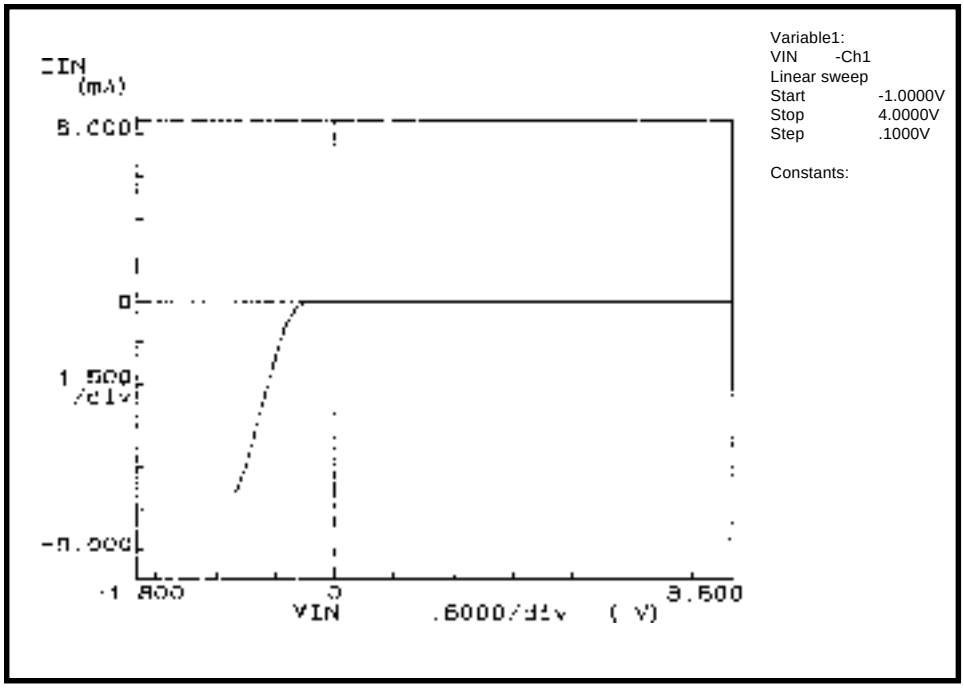


Figure 9. ispGDX Output Power-Up Characteristics

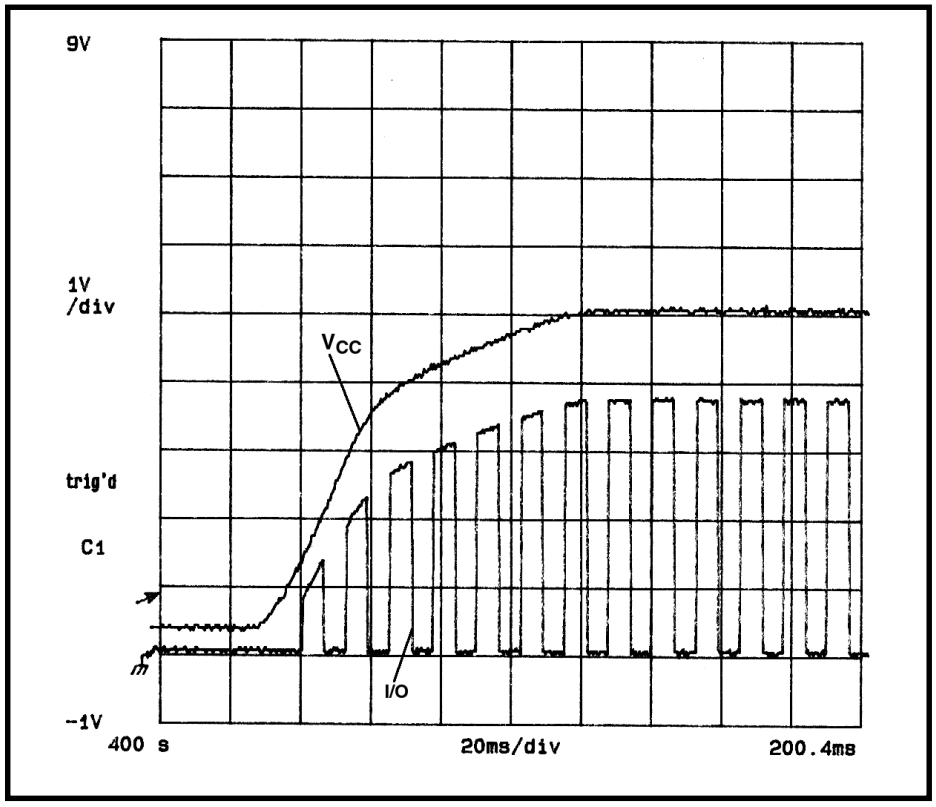


Figure 10. ispGDX Output Power-Down Characteristics

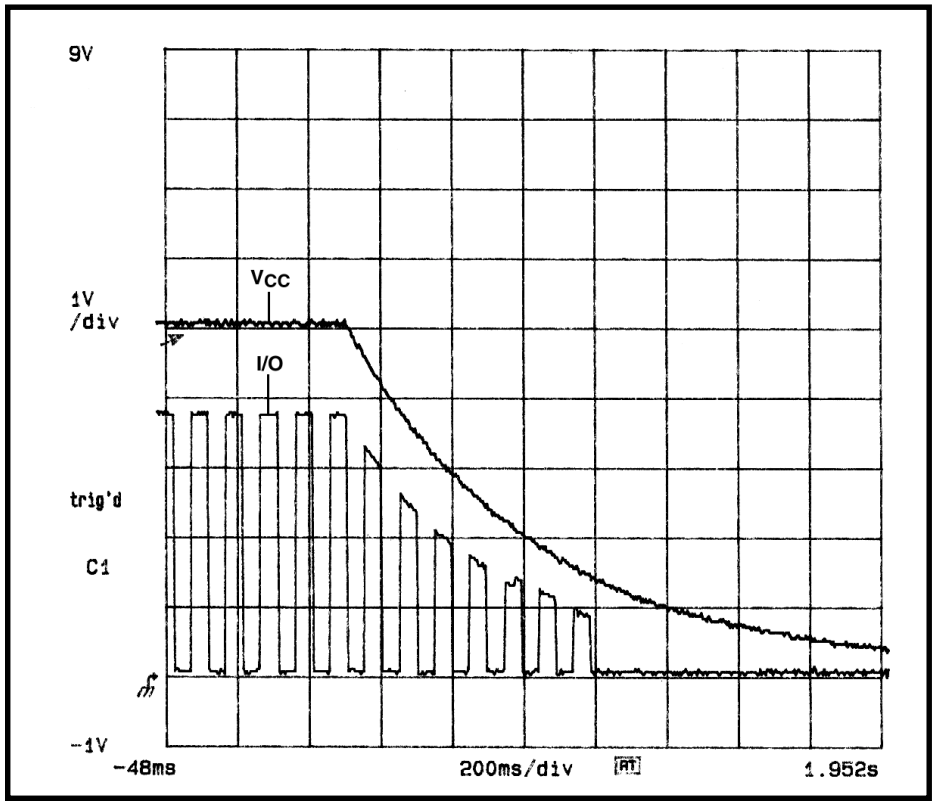


Figure 11. ispGDXV Output Power-up Characteristics

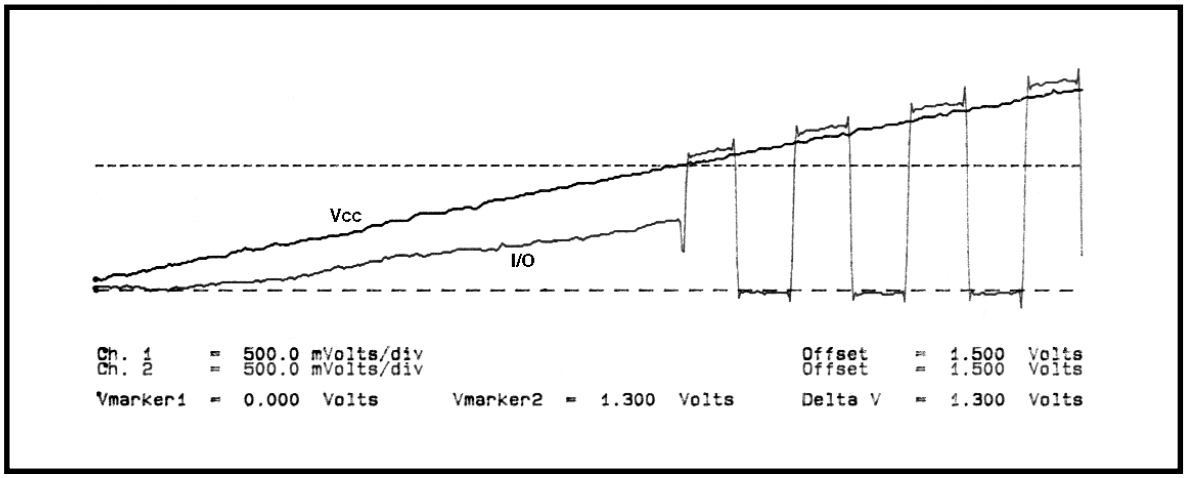


Figure 12. ispGDXV Output Power-down Characteristics

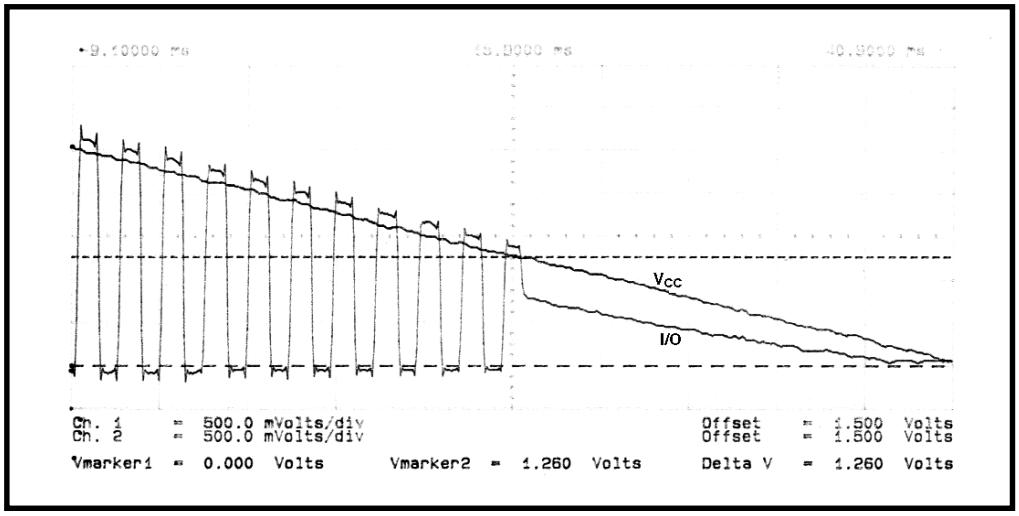


Figure 13. ispLSI 2000VE Output Power-up Characteristics

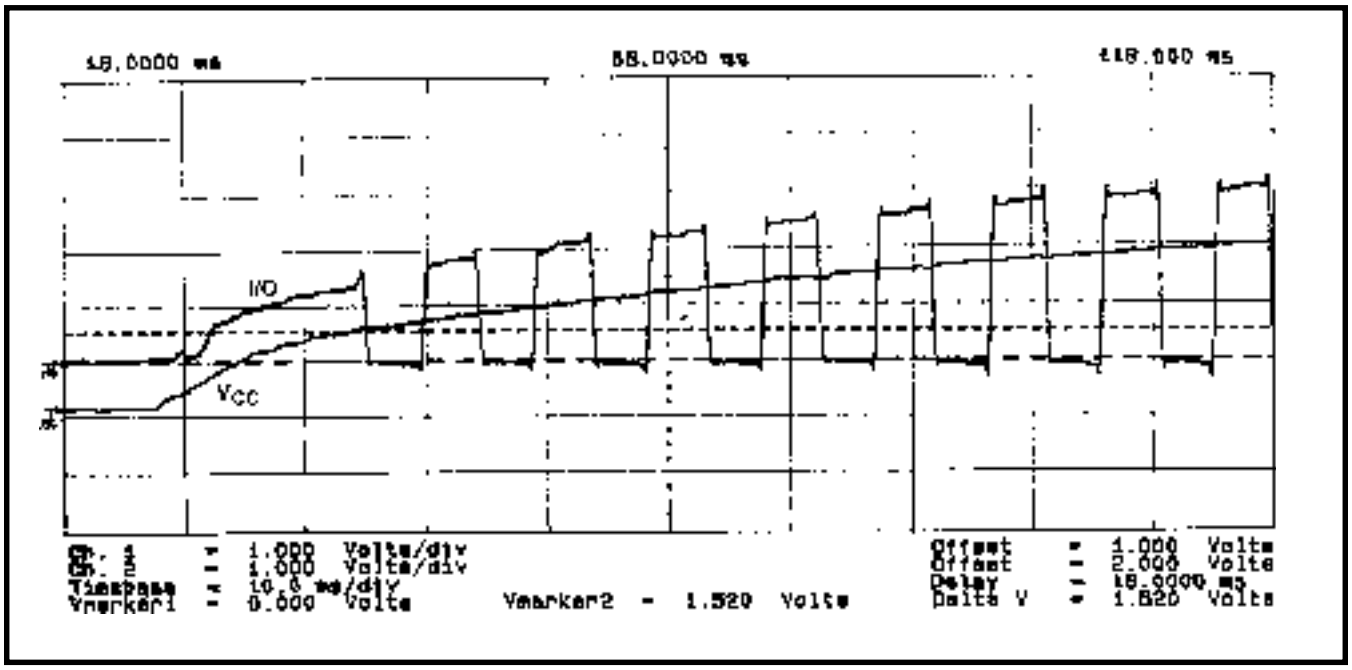


Figure 14. ispLSI 2000VE Output Power-down Characteristics

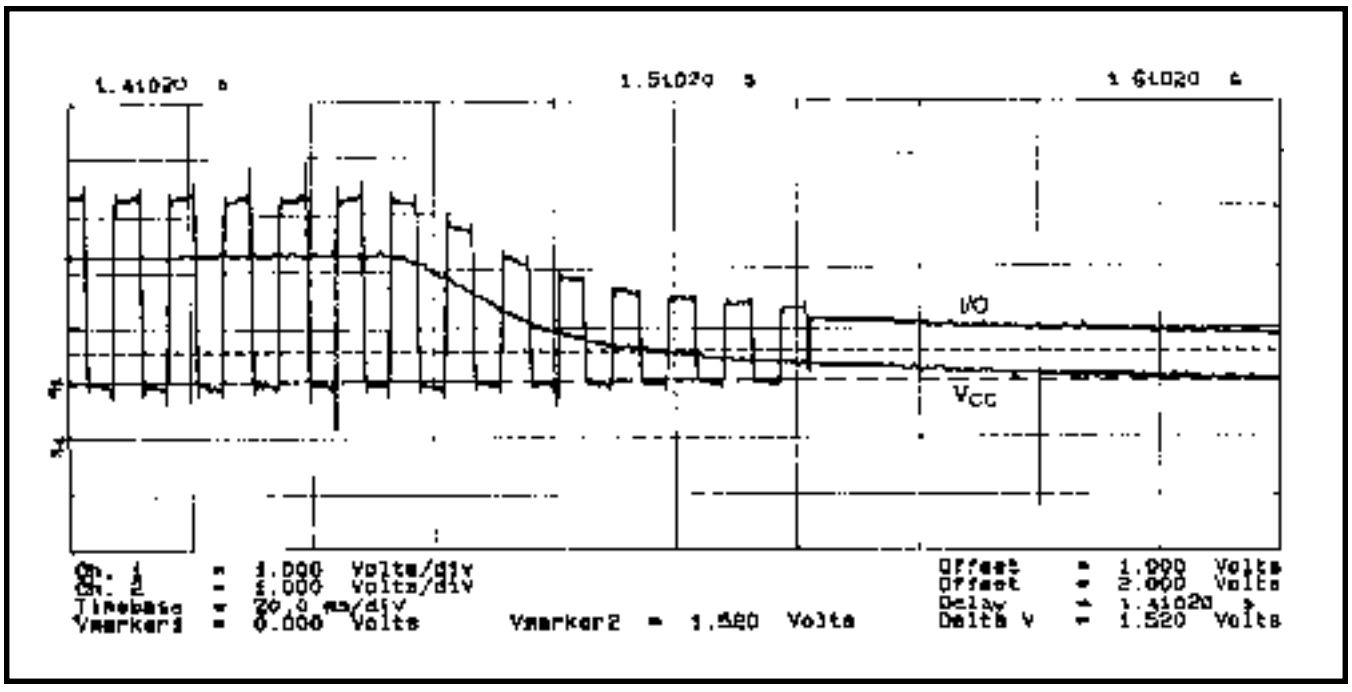


Figure 15. ispLSI 5000V Output Power-up Characteristics

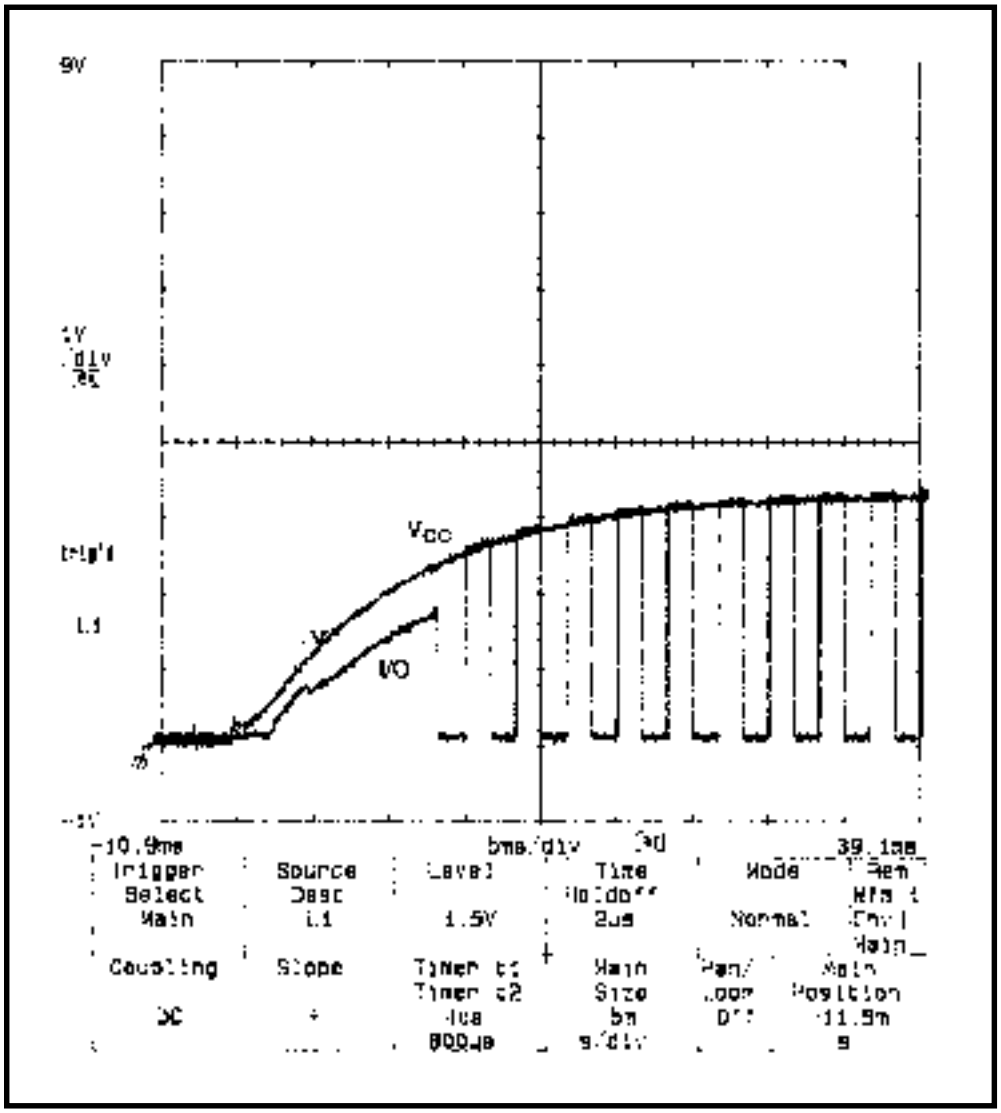


Figure 16. ispLSI 5000V Output Power-down Characteristics