ispGDX2

High Performance Digital Crosspoint Switch

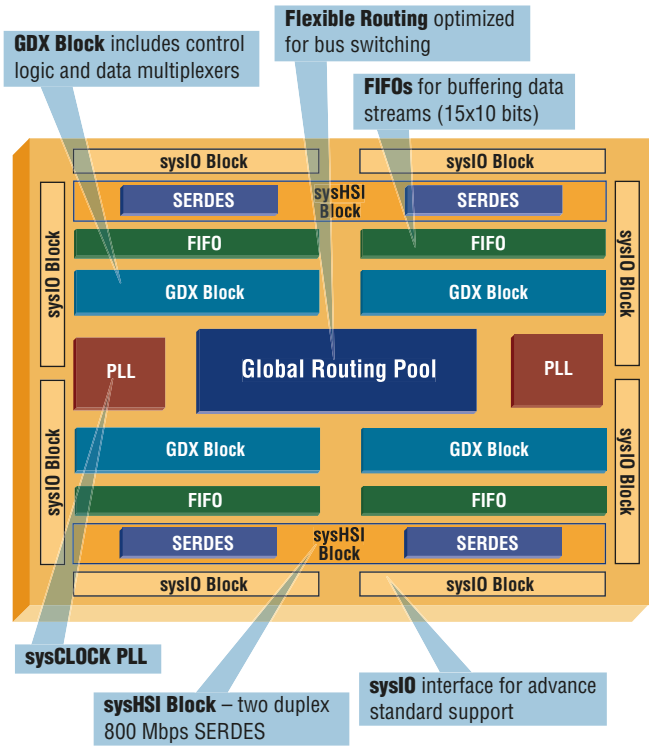
Fast Serial I/O and High Bandwidth Bus Interface

The ispGDX2™ family is Lattice's next generation in-system programmable (ISP™) high performance digital crosspoint switch for high-speed bus switching and interfacing with bandwidth of up to 38Gbps. This family combines a flexible switching architecture with advanced high speed serial I/O (sysHSI™ blocks), sysCLOCK™ PLLs, and sysIO™ interfaces to meet the needs of today's high-speed systems. A multiplexer based architecture and on-chip control logic facilitate the high performance implementation of common switching functions.

ispGDX2 devices are provided in 3.3V, 2.5V or 1.8V core voltage versions and can be programmed in-system via an IEEE 1149.1 interface that is compliant with the IEEE 1532 standard. Voltages required for the I/O buffers are independent of the core voltage supply. This further enhances the design flexibility of the family. Typical applications for the ispGDX2 include multi-port multi-processor interfaces, serial backplanes, wide data and address bus multiplexing, programmable control signal routing and programmable bus interfaces.

The ispGDX2 family is available in two options. The standard device supports sysHSI capability for ultra fast serial communications and the "E" series, a high performance, low cost device with no sysHSI functionality.

ispGDX2-64 Block Diagram



Key Features and Benefits

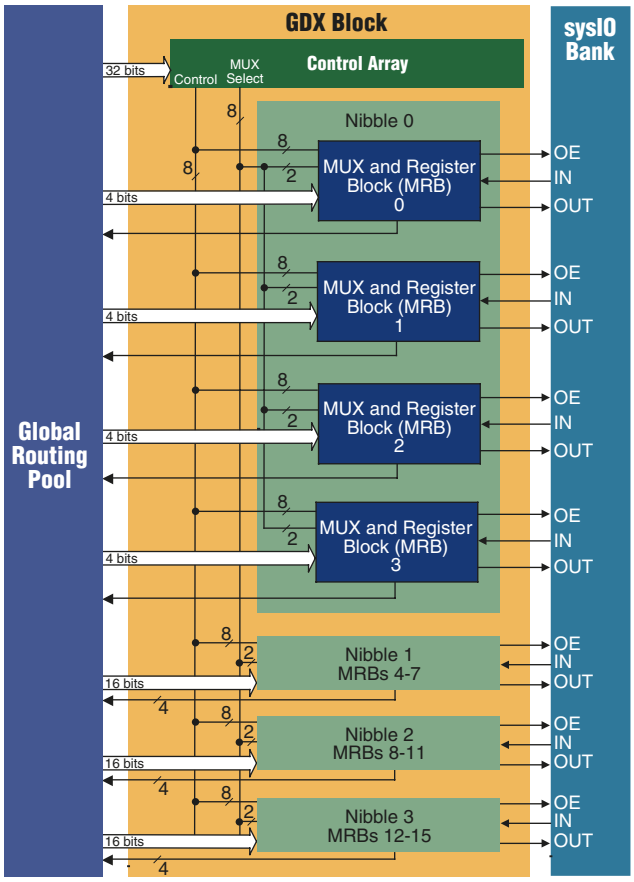
- **High Performance Bus Switching**
  - 12.8 Gbps (SERDES), 38 Gbps (without SERDES)*
  - Up to 16 (15X10) FIFOs for data buffering
  - High-speed Performance: f_{MAX} = 360 MHz, t_{PD} = 3.0ns
  - I/O intensive: 64 to 256 I/Os
  - Expanded MUX capability up to 188:1 MUX
- **sysCLOCK PLL**
  - Frequency synthesis and skew management
  - Clock shifting, multiply and divide capability
  - Jitter as low as 150ps
  - Up to four PLLs
- **sysIO Interfacing**
  - LVCMOS 1.8, 2.5, 3.3 and LVTTL support
  - SSTL 2/3 Class I and II support
  - HSTL Class I, III and IV support
  - GTL+, PCI-X support
  - LVPECL, LVDS and Bus LVDS support
  - Hot socketing
- **Up to 16 Channels of 800Mbps sysHSI SERDES**
  - Serializer/de-serializer (SERDES) included
  - Built-in Clock Data Recovery (CDR)
  - 10B/12B support
    - Encoding / decoding
    - Sync pattern support
    - Symbol alignment
  - 8B/10B support
    - Sync pattern support
    - Symbol alignment
  - Source synchronous capability
- **Flexible Programming & Testing**
  - IEEE 1532 compliant ISP
  - Boundary Scan test through IEEE 1149.1 Interface

** Bandwidth assumes 50% of I/Os are inputs and 50% are outputs.*

ispGDX2 Architecture

GDX Block

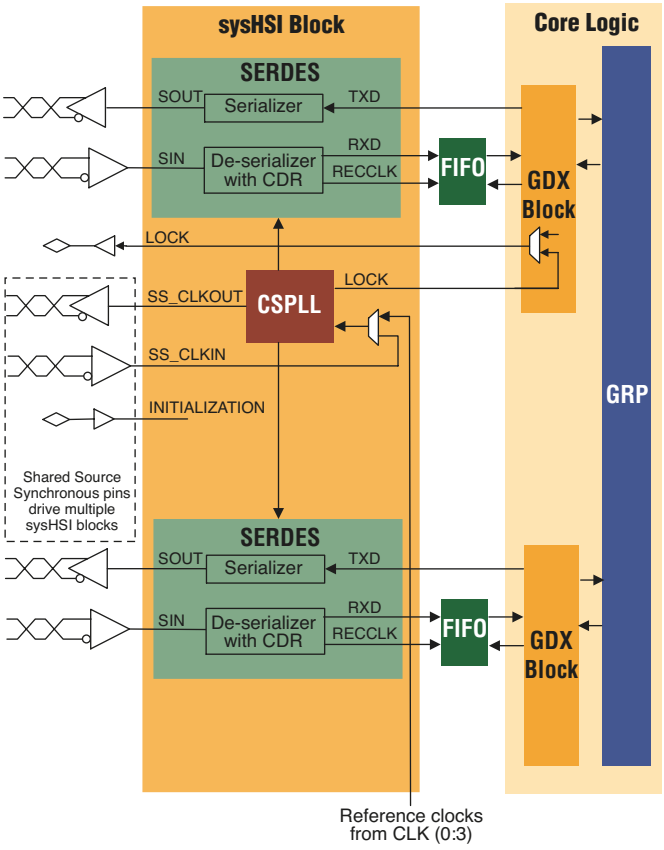
- 4 to 16 GDX Blocks per device
- 16 4:1 MUX and Register Blocks (MRBs) optimized for bus switching
- Separate registers for input, output, and output enable
- 32 input programmable control array provides block-level MUX select, clock, set/reset and output enable



sysHSI – High Speed Interface[1]

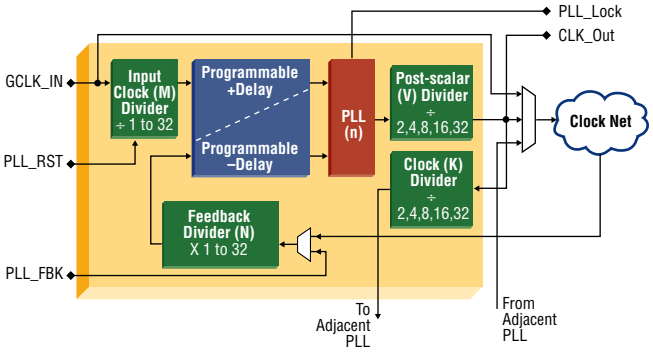
- 2 to 8 sysHSI Blocks per device
- Each sysHSI includes two 800 Mbps duplex SERDES (with CDR)
- Multiple sysHSI Blocks can be combined for source synchronous operation

1. Not available in the "E" series devices.



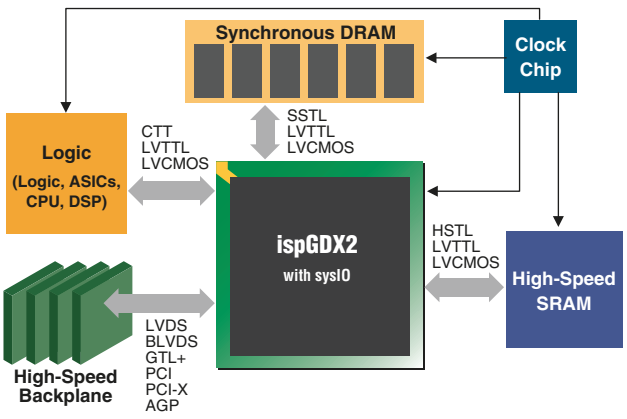
sysCLOCK PLL for Timing Control

- 2 to 4 sysCLOCK PLLs per device
- 10 to 320 MHz PLL operation
- PLL with period jitter of ±150ps



sysIO Interfaces

- On-board sysIO Banks allow ispGDX2 devices to support a wide range of I/O standards
- 8 sysIO Banks per ispGDX2 device
- Each sysIO Bank has its own separate I/O supply voltage and reference voltage

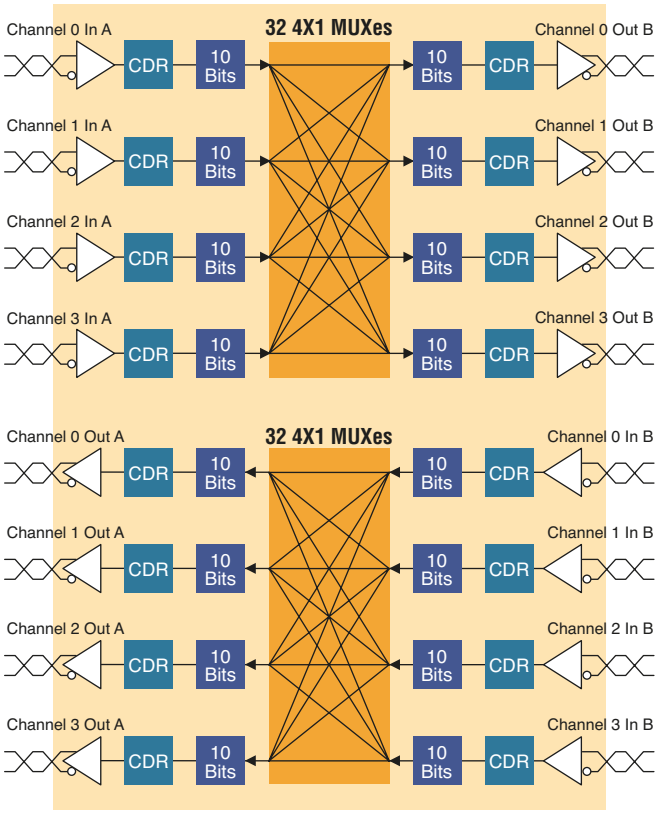


ispGDX2 Applications

4X4 Serial High-Speed Switch

The high performance architecture of the ispGDX2 is perfect for implementing crosspoint switches with multiple devices. In this application, the ispGDX2 device performs:

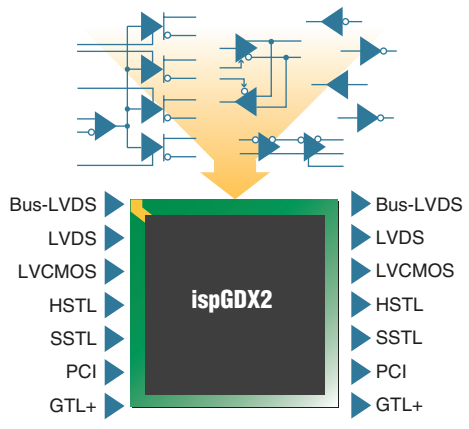
- Bi-directional 4X4 serial high-speed switches
- Bus-LVDS enables bigger crosspoint switches with multiple devices



Flexible I/O Buffer

The ispGDX2 provides a flexible method to integrate multiple buffers into a single device. ispGDX2 devices provide:

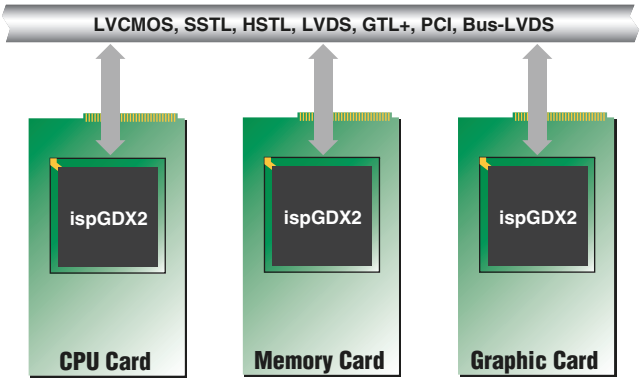
- Support for multiple standards
- In-system programmability and JTAG testability



Flexible High-Speed Backplane Driver

The sysIO capability of the ispGDX2 provides flexility in implementing backplane drivers. In the application below, the ispGDX2 devices provide the following features:

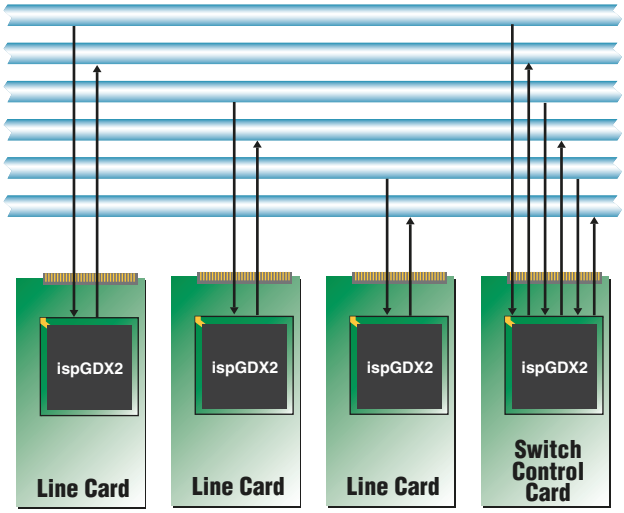
- Up to 38 Gbps bandwidth per ispGDX2 device
- In-system programmability and JTAG at board edge



Multi-Gigabit Serial Switched Backplane

The ispGDX2 offers a superior solution for signal routing and switching across backplanes. In the application below, the ispGDX2 devices provide the following features:

- One part type for implementing high-speed circuits on both line card and switch board
- Up to 12.8 Gbps bandwidth per ispGDX2
- Easy board side interface using sysIO and sysCLOCK features



ispGDX2 Family Attributes

Feature	ispGDX2-64/E[1]	ispGDX2128[2]/E[1]	ispGDX2-256/E[1]
I/Os	64	128	256
GDX Blocks	4	8	16
t_{PD}	3.0 ns	3.2 ns	3.5 ns
t_S	2.0 ns	2.0 ns	2.0 ns
t_{CO}	2.9 ns	3.1 ns	3.2 ns
f_{MAX}	360 MHz	330 MHz	300 MHz
Max. Bandwidth (SERDES)	3.2 Gbps	6.4 Gbps	12.8 Gbps
Max. Bandwidth (without SERDES)	11 Gbps	21 Gbps	38 Gbps
sysHSI Channels	4	8	16
Bus LVDS (Pairs)	32	64	128
PLLs	2	2	4
Package	100-Ball fpBGA	208-Ball fpBGA	484-Ball fpBGA

1. "E" series does not support sysHSI.
2. Preliminary information.

ispGDX2 Advanced Packaging

Packages are shown actual size. Dimensions refer to package body size.

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