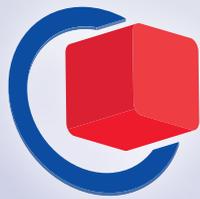


Nuremberg, Germany  
10.-12.3.2026



# embeddedworld

Exhibition & Conference

## CONFERENCE PROGRAM

[www.embedded-world.eu](http://www.embedded-world.eu)

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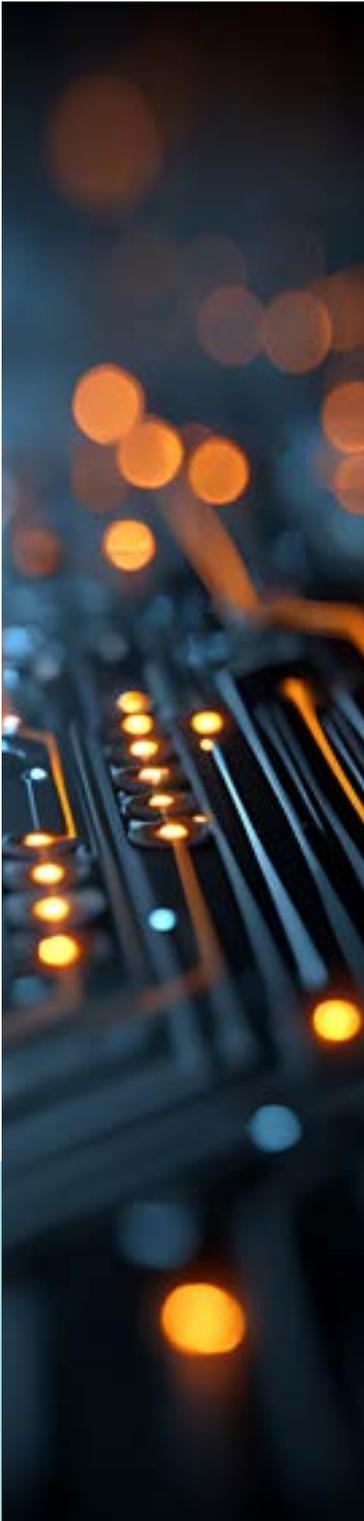
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WNDRVR



## The Dependable Foundation for Mission-Critical Edge AI Systems



Embedded engineers are being asked to run advanced AI workloads without compromising real-time performance, safety, or emerging compliance requirements. Wind River provides the deterministic software foundation, safety capabilities, open infrastructure, and lifecycle tools needed to build and operate autonomous and intelligent systems, reliably and at scale.

What this means for embedded engineers:



Real-time predictability even with AI workloads



Functional safety foundations for critical systems



Lifecycle orchestration and observability for easier updates and compliance readiness



Unified edge AI platform that reduces integration effort and avoids lock-in

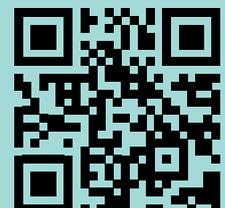
### Visit Us at Embedded World 2026

Nuremberg, Germany | March 10–12, 2026 | Booth 4-112

**Discover what's next for real-time edge AI at Embedded World 2026.**

See demonstrations and explore how engineers are building mission-critical autonomous systems – including support for navigating new European requirements such as the Cyber Resilience Act.

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Prof. Dr.-Ing. Axel Sikora  
Chairman of embedded world Conference

## **embedded world Conference 2026** **connecting the embedded community**

Welcome to the 24<sup>th</sup> edition of embedded world Exhibition & Conference scheduled in Nuremberg during 10 - 12 March 2026! The **unique combination** of an exhibition for engineers and technical management and a world-leading conference at the intersection of applied research and industrial applications has proven extremely successful. embedded world is **driven by technology** as well as by applications with a strong focus on **system and cross domain aspects**.

Our slogan "connecting the embedded community" recognizes three aspects of the event:

- It is great to host a global event in Nuremberg that's experiencing a roaring increase in international speakers and visitors from all continents. This goes along with the growing international presence of the embedded world. Since 2023, we had three top class and very busy editions of embedded world Exhibition & Conference China in Shanghai; and since 2024, two editions of embedded world Exhibition & Conference North America in Austin (Texas, 2024) and Anaheim (California, 2025). There is more to come to grow the international footprint.
- embedded world 2026 will cover all aspects of the development and application of embedded systems, from fundamental technologies to development processes and special fields of applications. It is one of the central strengths of the event to be cross-sectoral and interdisciplinary. The conference provides a platform to bring together experts from different domains and application areas of embedded systems in order to promote a holistic system design perspective, to identify synergies and commonalities, and to strengthen the exchange of knowledge and experiences.

One key element here is the close collaboration with our community partners, who help us in coping with today's complexity of dependable embedded systems of systems. We organized and are running special sessions with alliances such as the Ambient IoT Alliance, Bluetooth SIG, CAN in Automation, CHERI Alliance, Eclipse Foundation, EDGE AI FOUNDATION, Edge AI & Vision Alliance, FED, MIPI Alliance, MISRA, RISC-V Foundation, SPE System Alliance, UCle, Yocto Project, Zephyr Project. This makes the embedded world truly a **community of communities**. We are grateful for this collaboration.

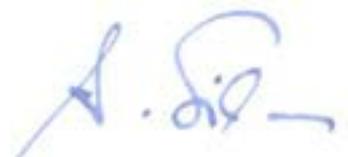
- Connecting embedded systems of systems and the Internet of Things, connecting people and things, and driving the embedded world to new levels – with regards to semiconductor technology, to algorithms, to signal processing. With regards to embedded systems, we are talking about connecting machines. With our embedded world event, we are connecting people and communities!

This 24<sup>th</sup> edition of the embedded world delivers a thrilling program **structured along eight tracks**. The program features a total of **218 hours** of knowledge delivery and exchange.

- The **81 sessions** with 243 **presentations** will integrate **Q&A** rounds between speakers and participants in each session.
- We will have a **keynote** from **Richard J. Simoncic, COO Microchip Technology**, who will talk on "**Learning from the Octopus: Nature's Blueprint for Intelligence Everywhere**", with Intelligence Everywhere being one of the hot topics of our industry.
- **20 half- or full day classes** will enable an in-depth knowledge transfer of current and relevant embedded systems topics.
- We will also feature **five expert panel discussions** on relevant overarching topics such as "Embedded Vision on the Rise", "Is RISC-V Ready for Automotive? Is Automotive Ready for RISC-V?", "Emerging Cybersecurity Strategies for Software-Defined Vehicles", or "Navigating the EU Cyber Resilience Act: From Policy to Practice". We will also have one panel "C-Level @ embedded world" with top notch industry leaders to discuss strategic questions of the embedded industry.

The steering board of embedded world 2026 wishes all participants stimulating discussions about new ideas and solutions enabling the community to more efficiently cope with the immense challenges that lie ahead for our industries and societies. We welcome you to gain great insights in a pulsating atmosphere.

It will be good to see all of you in Nuremberg ... and in Shanghai ... and in Anaheim...!



Prof. Dr.-Ing. Axel Sikora  
Chairman of embedded world Conference



Tuesday, 10 March 2026, 10:00, NCC Ost, Level 3, Room TOKIO

**Conference Keynote**

**Learning from the Octopus: Nature’s Blueprint for Intelligence Everywhere**

Consider the octopus: two-thirds of its neurons are distributed throughout its tentacles and skin, enabling each to sense, decide, and act independently – an evolutionary strategy for intelligence that is both resilient and efficient. In the embedded world, we have long recognized the value of distributed intelligence. Today, as we scale to tens of billions of connected devices, the challenges and opportunities of managing power, integration complexity, and future security threats are more relevant than ever.

The keynote will share how nature’s blueprint can benefit the industry’s collective journey; moving beyond centralized “brains” to intelligent, secure, and sustainable nervous systems at every touch point. It will address key technical considerations and discuss approaches to managing development costs and resource allocation, the importance of industry standards and collaboration, and the necessity of comprehensive support and training for engineering teams.

The future of AI belongs not to those who build the biggest brains, but to those who build the most adaptive, secure, and distributed systems, just as nature has done for millions of years.

**Richard J. Simoncic**

Richard J. Simoncic joined Microchip in 1989 and became COO in April 2024. Mr. Simoncic oversees Microchip’s worldwide operations and is leading the company’s AI-related efforts.

He founded Microchip’s internal analog business in 1998, growing it to over \$2 billion in annual revenue. Mr. Simoncic previously held roles as Executive Vice President (2023), Senior Vice President (2019-2023), and Vice President (1995-2019).

Mr. Simoncic holds a B.S. in Electrical Engineering Technology from DeVry Institute of Technology.

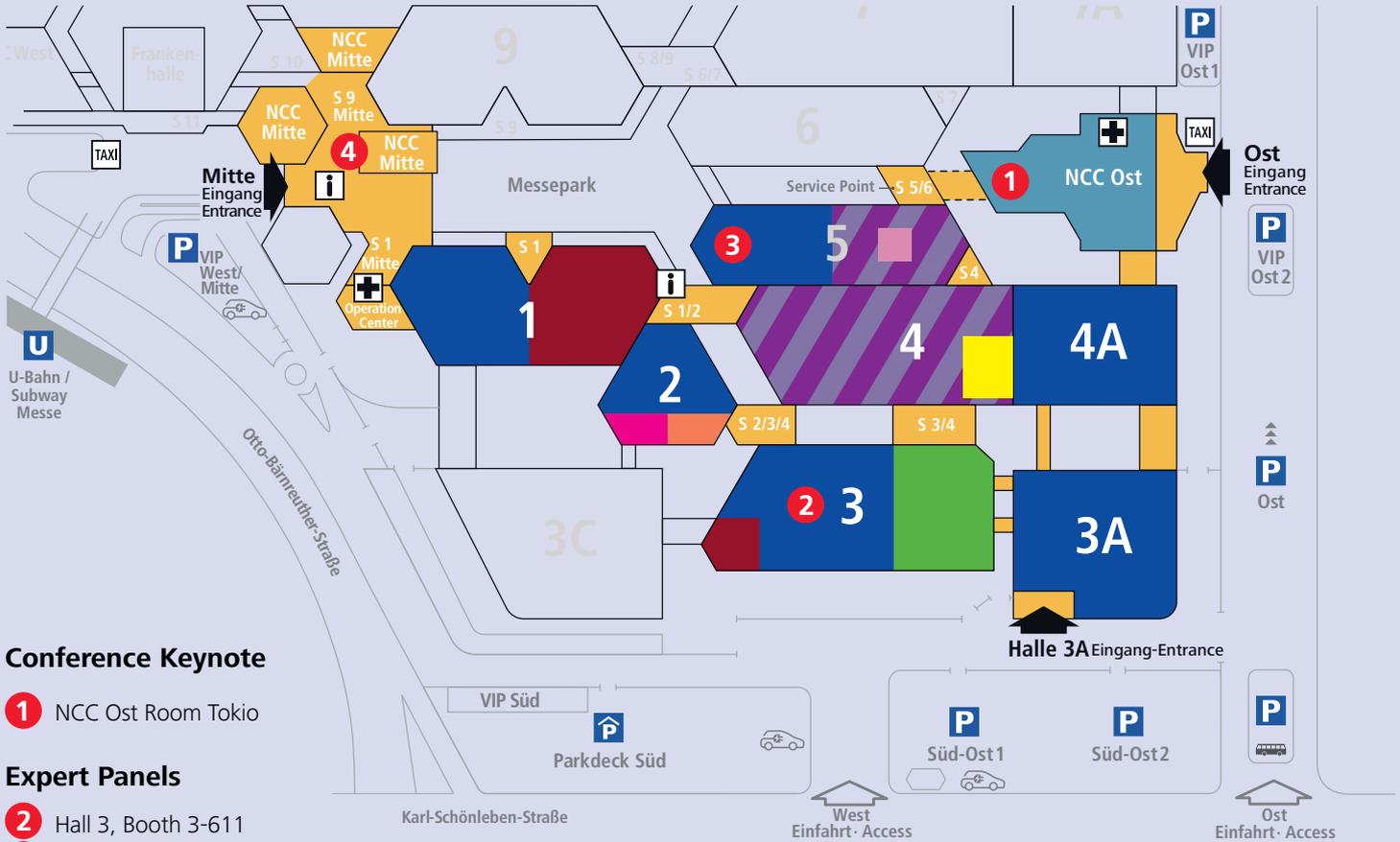


The photo was taken at the Offenburg University of Applied Sciences, Germany.

**STEERING BOARD**

*(from left to right):*  
Prof. Dr. Dirk Pesch,  
Dr. Bernd Hense,  
Caspar Grote,  
Prof. Dr. Axel Sikora,  
Prof. Dr. Peter Fromm,  
Prof. Dr. Ansgar Meroth.

The steering board is the strategic think tank behind the embedded world Conference. Currently six senior engineers with excellent scientific and business records, with open minds and a lot of ideas, shape the future direction of the embedded world Conference.



**Conference Keynote**

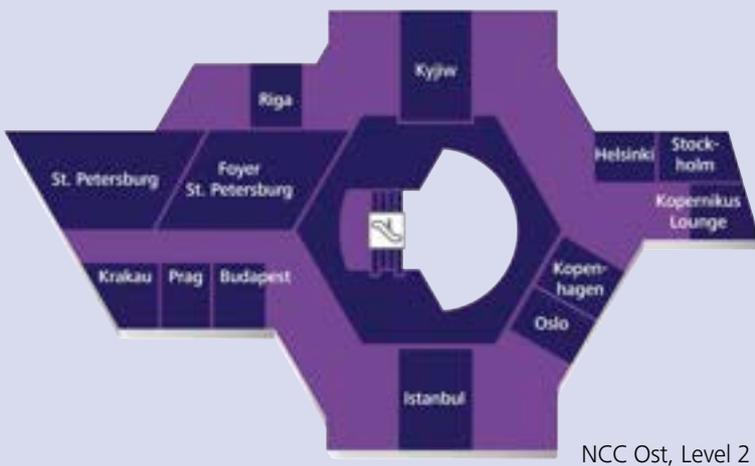
- 1** NCC Ost Room Tokio

**Expert Panels**

- 2** Hall 3, Booth 3-611
- 3** Hall 5, Booth 5-210

**Student Day**

- 4** NCC Mitte, Room Brüssel



## CONFERENCE PROGRAM

Tuesday, 10 March

Wednesday, 11 March

9:30 - 13:00	Class 2.1 <b>Faster. Smarter. Firmware.</b> Modern Best Practices for Better Embedded Systems Room Helsinki	Class 2.2 <b>Hands-On Zephyr Project Workshop</b> Room Neu-Delhi	Class 4.1 <b>Soft Logic, Hard Math: Building a RISC-V FPU With IEEE 754 Support on FPGAs</b> Room Singapur	Class 7.1 <b>Introduction to tinyML – Deploying Deep Learning Models Onto Low-power Micro-Controllers</b> Room Krakau	Class 3.1 <b>CRA Regulations and Certification</b> Room Singapur	Class 5.3 <b>Programming With Rust for C/C++ Programmers</b> Room Neu-Delhi
14:00 - 17:00	Class 4.2 <b>Safeguarding Industrial Interfaces: Reliable Protection Against Transient Overvoltage</b> Room Helsinki	Class 5.1 <b>Rust, a Safe Language for Low-level Programming</b> Room Neu-Delhi	Class 5.2 <b>GitLab for Embedded DevOps: Integrated AI for Both DevSecOps Adoption and Product Delivery</b> Room Singapur	Class 7.2 <b>Edge AI: Evolution and Hands-on</b> Room Krakau	Class 2.3 <b>Embedded GNU/Linux in Mid-integrity/ Mixed-criticality Safety-related Systems</b> Room Neu-Delhi	Class 2.4 <b>Embedded Linux Security Exercised on the Secure Platform GyroidOS</b> Room Singapur

	1. IOT & CONNECTIVITY	2. EMBEDDED OS	3. SAFETY & SECURITY	4. HARDWARE DESIGN		
<b>DAY 1</b>	Session 1.1 <b>Ambient IoT</b> (powered by Ambient IoT Alliance) Room Kopenhagen	Session 1.4 <b>WiFi and Long-Range</b> Room Stockholm	Session 2.1 <b>Long-Term Stability with Yocto</b> (powered by Yocto Project) St. Petersburg	Session 3.1 <b>Implementing the Cyber Resilience Act (CRA)</b> Room Istanbul	Session 3.4 <b>Open Source for Safety &amp; Security 1</b> Room Oslo	Session 4.1 <b>Chiplets in Automotive Applications</b> (powered by UCIe) Room Budapest
	Session 1.2 <b>IoT Ecosystem Technologies 1</b> Room Kopenhagen	Session 1.5 <b>CAN Technologies</b> (powered by CiA) Room Stockholm	Session 2.2 <b>Yocto Use Cases</b> (powered by Yocto Project) St. Petersburg	Session 3.2 <b>Post Quantum Cryptography Strategies</b> Room Istanbul	Session 3.5 <b>Open Source for Safety &amp; Security 2</b> Room Oslo	Session 4.2 <b>Chiplets - Certification, Validation &amp; Test</b> (powered by UCIe) Room Budapest
	Session 1.3 <b>IoT Ecosystem Technologies 2</b> Room Kopenhagen	Session 1.6 <b>CAN Safety &amp; Security</b> (powered by CiA) Room Stockholm	Session 2.3 <b>RTOS Orchestration</b> St. Petersburg	Session 3.3 <b>Long-Term &amp; Post Quantum Security</b> Room Istanbul	Session 3.6 <b>Trusted Artificial Intelligence</b> Room Oslo	Session 4.3 <b>MIPI Interfaces</b> (powered by MIPI Alliance) Room Budapest
<b>DAY 2</b>	Session 1.7 <b>Ethernet Time Sensitive Networking (TSN)</b> Room Kopenhagen	Session 1.10 <b>Cellular - Emerging Technologies</b> Room Stockholm	Session 2.4 <b>Zephyr - Best Practice</b> (powered by Zephyr Project) St. Petersburg	Session 3.7 <b>Reliable Architectures</b> Room Istanbul		Session 4.4 <b>System on Chip Design Process</b> Room Budapest
	Session 1.8 <b>Single-Pair Ethernet</b> (powered by SPE System Alliance) Room Kopenhagen	Session 1.11 <b>Cellular - 5G</b> Room Stockholm	Session 2.5 <b>Zephyr in Safety-Critical Applications</b> (powered by Zephyr Project) St. Petersburg	Session 3.8 <b>Reliable Code / Safe Rust</b> Room Istanbul		Session 4.5 <b>System Hardware - Design Examples</b> Room Budapest
	Session 1.9 <b>Applying Ethernet Technologies</b> Room Kopenhagen	Session 1.12 <b>Cellular - eSIM</b> Room Stockholm	Session 2.6 <b>Zephyr Use Cases</b> (powered by Zephyr Project) St. Petersburg	Session 3.9 <b>Reliability Testing</b> Room Istanbul		Session 4.6 <b>Architectural Design</b> Room Budapest
<b>DAY 3</b>	Session 1.13 <b>Bluetooth - Best Practices</b> (powered by Bluetooth SIG) Room Kopenhagen		Session 2.7 <b>Container Use Cases</b> St. Petersburg	Session 3.10 <b>Ensuring Resilient Embedded Systems</b> Room Istanbul		Session 4.7 <b>Hardware Design and Production Process</b> (powered by FED) Room Budapest
	Session 1.14 <b>Bluetooth - Emerging Technologies</b> (powered by Bluetooth SIG) Room Kopenhagen		Session 2.8 <b>Beyond Virtualization</b> St. Petersburg	Session 3.11 <b>DevSecOps for Safe &amp; Secure Systems</b> Room Istanbul		Session 4.8 <b>Hardware Design Examples</b> Room Budapest
	Session 1.15 <b>Bluetooth in Automotive Applications</b> (powered by Bluetooth SIG) Room Kopenhagen		Session 2.9 <b>Real-Time Virtualization</b> St. Petersburg	Session 3.12 <b>Trustworthy Systems with CHERI &amp; RISC-V</b> (powered by CHERI Alliance) Room Istanbul		Session 4.9 <b>Power Supply Design</b> Room Budapest

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**CONFERENCE PROGRAM**
**Wednesday, 11 March**
**Thursday, 12 March**

Class 5.4 <b>C++ and Modern C++ for Embedded Development</b> Room Krakau	Class 7.3 <b>From Vision to Deployment: Developing Secure AI-Enabled Linux Devices</b> Room Helsinki	Class 2.5 <b>Introduction to Embedded Linux Using a Yocto Project SDK</b> Room Neu-Delhi	Class 4.3 <b>FPGA-Design Using C/C++ and High-Level Synthesis</b> Room Helsinki	Class 4.4 <b>Designing Battery-free IoT</b> Room Krakau	Class 5.5 <b>Embedded Software Testing – With Fundamental Skills and Artificial Intelligence</b> Room Singapur
Class 3.2 <b>Cyber Resilience Act (CRA) – Practical Implementation Examples</b> Room Krakau	Class 3.3 <b>Embedded Safety Architectures</b> Room Helsinki				

	5. SOFTWARE & SYSTEMS ENGINEERING	6. EMBEDDED VISION	7. EDGE AI	8. USE CASES FOR EMBEDDED
	Session 5.1 <b>Programming Languages: Rust</b> Room Kiew	Session 5.4 <b>Software Architectures</b> (powered by Eclipse Foundation) Room Riga	Session 6.1 <b>Concepts and Standards</b> Room Prag	
	Session 5.2 <b>Programming Languages</b> Room Kiew	Session 5.5 <b>Development Processes for Software Defined Vehicles (SDV)</b> Room Riga	Session 6.2 <b>Hardware Acceleration</b> Room Prag	
	Session 5.3 <b>MISRA SW-Coding Guidelines</b> (powered by MISRA) Room Kiew	Session 5.6 <b>Open Source Software</b> Room Riga	Session 6.3 <b>Pipelines</b> (powered by Edge AI & Vision Alliance) Room Prag	
	Session 5.7 <b>Testing Embedded Software</b> Room Kiew		Session 6.4 <b>Emerging Embedded Vision and Audio Technologies</b> Room Prag	Session 7.1 <b>Lightweight Embedded AI</b> Room Riga
	Session 5.8 <b>Trustable Embedded Software</b> Room Kiew		Session 6.5 <b>EV Use Cases</b> Room Prag	Session 7.2 <b>Neuromorphic Computing</b> Room Riga
	Session 5.9 <b>Formal Verification</b> Room Kiew		Session 6.6 <b>Radar and Artificial Intelligence</b> Room Prag	Session 7.3 <b>Qualification and Validation</b> Room Riga
Session 4.10 <b>RISC-V Ecosystem</b> (powered by RISC-V Foundation) Room Stockholm	Session 5.10 <b>DevOps &amp; CI/CD Pipeline</b> Room Kiew	Session 5.13 <b>Digital Twin</b> Room Riga		Session 7.4 <b>Execution</b> Room Prag
Session 4.11 <b>RISC-V Applications</b> (powered by RISC-V Foundation) Room Stockholm	Session 5.11 <b>Workflows and Tools</b> Room Kiew	Session 5.14 <b>Software Debugging and Tracing</b> Room Riga		Session 7.5 <b>From Lab to Field</b> Room Prag
Session 4.12 <b>Open-Source SoC Hardware</b> Room Stockholm	Session 5.12 <b>Technical Debt and Legacy</b> Room Kiew	Session 5.15 <b>Generating Flexible &amp; Efficient Code</b> Room Riga		Session 7.6 <b>Use Cases</b> (powered by EDGE AI FOUNDATION) Room Prag
				Session 8.1 <b>Medical Applications</b> Room Oslo
				Session 8.2 <b>Predictive Maintenance Applications</b> Room Oslo
				Session 8.3 <b>Mobility Applications</b> Room Oslo
				Session 8.4 <b>Development Processes</b> Room Oslo
				Session 8.5 <b>Security Applications 1</b> Room Oslo
				Session 8.6 <b>Security Applications 2</b> Room Oslo

Community Partners



Ambient IoT Alliance



**Class 2.1** 10.03.2026, 9:30 – 13:00

**Faster. Smarter. Firmware. Modern Best Practices for Better Embedded Systems**

*Jacob Beningo, Beningo Embedded Group*

Most firmware development teams spend thousands of dollars per engineer in lost productivity from late projects, rework, and quality issues. This class is designed to pay for itself many times over by giving your team the frameworks and practices to deliver faster, smarter, and more reliable firmware. You'll leave with a clear roadmap and practical techniques you can apply immediately.

**Class 2.2** 10.03.2026, 9:30 – 13:00

**Hands-On Zephyr Project Workshop**

*Jonas Remmert, SMIGHT*

This class helps embedded developers explore the Zephyr Project, focusing on IoT development through simulation and hands-on exercises that guide attendees through command-line interactions, modular application building with ZBus, and testing strategies using Twister and native simulation. Participants will build foundational knowledge of Zephyr and engage in practical examples. No physical hardware is required, emphasizing virtualized environments.

**Class 4.1** 10.03.2026, 9:30 – 13:00

**Soft Logic, Hard Math: Building a RISC-V FPU With IEEE 754 Support on FPGAs**

*Marc Honman, Altera*

Adding IEEE 754 floating-point support to an embedded-class processor presents a complex trade-off between performance, area, and implementation effort. This class explores these challenges through the design of an FPU for the NiosV processor (RISC-V RV32F), targeting FPGA platforms with hardened DSP blocks and vendor-provided soft floating-point primitives.

**Class 7.1** 10.03.2026, 9:30 – 13:00

**Introduction to tinyML – Running Deep Learning Models on Low-Power Microcontrollers**

*Prof. Daniel Mueller-Gritschneider, Technische Universität Wien*

An in-depth introduction to tinyML, the field of deploying machine learning (ML) models on resource-constrained edge devices like MCUs and sensors. Participants will learn the full pipeline of developing efficient ML models optimized for low-power, low-memory environments. This class covers the essential stages like model preparation, model evaluation, and finally code generation.

**Class 4.2** 10.03.2026, 14:00 – 17:00

**Safeguarding Industrial Interfaces: Reliable Protection Against Transient Overvoltage**

*Dr. Heinz Zenkner, Würth Elektronik eiSos*

This class addresses the robust protection of industrial interfaces against transient overvoltages without degrading high-speed signal performance – by combining RF-filters and surge protection components. It details the operation of TVS diodes, Metal-oxide varistors, and gas discharge tubes – including application examples, component selection, filter integration, and PCB layout tips.

**Class 5.1** 10.03.2026, 14:00 – 17:00

**Rust, a Safe Language for Low-level Programming**

*Prof. Dr. Stefan Wehr, Hochschule Offenburg*

Main goals of the Rust language are performance, correctness, safety and productivity. Rust provides 100% memory safety and safety against data races, plus some features known from high-level languages: immutability, algebraic data types, pattern matching, traits and closures – and its performance is comparable with C or C++. After an introductory talk explaining the main concepts behind Rust, this half-day class equips attendees with practical experience in Rust through various exercises.

**Class 5.2** 10.03.2026, 14:00 – 17:00

**GitLab for Embedded DevOps: Integrated AI for Both DevSecOps Adoption and Product Delivery**

*James Moverly, GitLab*

The adoption of a new RTOS or hardware is a great time for greater alignment of your Embedded SDLC with DevOps. This class, targeting developers and development managers looking to leverage the value promises of DevOps with security and compliance, is technical but also shows how to ramp up your organization's modernization of the Embedded SDLC, discussing all details required for this process.

**Class 7.2** 10.03.2026, 14:00 – 17:00

**Edge AI: Evolution and Hands-on**

*Danilo Pietro Pau, STMicroelectronics*

This class covers AI milestones from an industry view, explaining Fixed AI origins and Edge AI meaning. It addresses the heterogeneity challenge at the edge and how unified AI core technology solves it across hardware like MCUs and sensors. The class also highlights generative AI advances at the edge, including practical demos on STM32MP2 and future outlooks. Participants get a good overview of the ST EdgeAI solutions required to design and deploy tinyML models on ST hardware boards.

**Class 3.1** 11.03.2026, 9:30 – 13:00

**CRA Regulations and Certification**

*Joe Lomako, TÜV SÜD*

This class is a concise introduction to the Cyber Resilience Act (CRA) to help manufacturers understand and prepare for this new legislation. We will explore the origins of the CRA, its reasoning and the scoping as compared to the RED directive, and provide detailed introductions into the essential requirements, overall obligations of manufacturers and authorized representatives – followed by guidance for manufacturers how to prepare their company for the transition points of the CRA.

**Class 5.3** 11.03.2026, 9:30 – 13:00

**Programming with Rust for C/C++ Programmers**

*Prof. Dr. Dieter Nazareth, Landshut University of Applied Sciences*

The modern programming language Rust offers memory safety without compromising performance, making it ideal for programming safety-critical systems. This class takes a critical look at Rust to decide whether replacing C/C++ with Rust brings benefits to your company, too. You will get an overview of the features and learn the main concepts of the language based on C/C++ knowledge.

**Class 5.4** 11.03.2026, 9:30 – 13:00**C++ and Modern C++ for Embedded Development***Dr. Carmelo Loiacono, Green Hills Software*

In this class, we will discuss the use of C++ and modern C++ for embedded development, focusing on its benefits and challenges. By the end of the class, participants will be able to apply key modern C++ features to embedded software development, follow best practices for writing safe, maintainable, and efficient embedded C++ code, and recognize how modern C++ concepts improve reliability and performance in resource-constrained environments..

**Class 7.3** 11.03.2026, 9:30 – 13:00**From Vision to Deployment:  
Developing Secure AI-Enabled Linux Devices***Raul Muñoz, Foundries.io*

This hands-on class targets embedded developers and AI engineers who want to bridge the gap between proof-of-concept and production. Attendees learn how to develop AI-powered embedded Linux devices with a robust, secure, and scalable lifecycle – all in just 3 hours, experiencing a full development workflow with Qualcomm-powered boards to combine the power of FoundriesFactory and Edge Impulse.

**Class 2.3** 11.03.2026, 14:00 – 17:00**Embedded GNU/Linux in Mid-integrity/Mixed-criticality Safety-related Systems***Nicholas Mc Guire, OSADL*

In this class, we examine the viability of employing IEC 61508 Ed2 for GNU/Linux in mid-integrity, mixed-criticality, safety-related systems – addressing challenges like certified multi-core hardware or continuous update of a complex software stack – and what compliance arguments/paths we see fit for mixed-criticality systems.

**Class 2.4** 11.03.2026, 14:00 – 17:00**Embedded Linux Security Exercised  
on the Secure Platform GyroidOS***Dr. Michael Weiß, et al., Fraunhofer AISEC*

This class shows how Linux can be used on embedded devices to comply with security related certification requirements like IEC 62443 or Common Criteria – focusing on security mechanisms provided by the Linux kernel. We will address mechanisms to protect the integrity of code and data and give practical insights into the implementation and usage of those mechanisms based on GyroidOS.

**Class 3.2** 11.03.2026, 14:00 – 17:00**Cyber Resilience Act (CRA) –  
Practical Implementation Examples***Dr. Norbert Paul, Hitex*

In this compact class, you will learn the basic implications of the CRA on embedded systems and gain the knowledge and tools you need to meet these challenges. Using real-world examples, you will learn the basics of Trustzone, Trusted Firmware, bootloaders, and related topics – plus the importance of individual steps in the development process for creating more secure applications.

**Class 3.3** 11.03.2026, 14:00 – 17:00**Embedded Safety Architectures***Alessandro Bastoni, STMicroelectronics*

This class focuses on safety-compliant designs based on MCUs and MPUs. Key embedded safety architectures developed in compliance with IEC 61508, ISO 13849, and ISO 26262 will be explained in detail, emphasizing the interrelationships between various aspects of safety compliance. We will also cover considerations for architecture selection such as achievable safety targets, availability, effective HW and SW partitioning, resulting requirements for main components, and other relevant factors.

**Class 2.5** 12.03.2026, 9:30 – 16:30**Introduction to Embedded Linux Using a Yocto  
Project SDK***Robert Berger, Reliable Embedded Systems*

This one-day training class uses hands-on exercises combined with instruction to illustrate some basic concepts of Embedded Linux. Hands-on sessions are performed on the host with a Yocto Project SDK and on some target hardware. The class provides the necessary practical experience to go ahead and configure/build an Embedded Linux system with mainline components.

**Class 4.3** 12.03.2026, 9:30 – 16:30**FPGA-Design Using C/C++ and High-Level Synthesis***Prof. Dr. Frank Kesel, Hochschule Pforzheim*

High-Level Synthesis (HLS) tools enable the implementation of algorithms coded in C/C++ as FPGA IP cores. HLS tools can quickly generate different RTL architectures and explore the tradeoff between performance and resource usage. Also, the generated VHDL/Verilog code can be easily verified using the C/C++ testbench. This hands-on workshop gives an introduction in the design of IP cores for Xilinx FPGAs using the Vivado HLS tool, from a design flow overview and the influence of data types to the use of directives and interpreting synthesis results.

**Class 4.4** 12.03.2026, 9:30 – 16:30**Designing Battery-free IoT***Herman Roebbers, Capgemini Engineering*

Let's make our IoT devices run without batteries! This full-day class will show how to design battery-free IoT devices by explaining energy saving techniques on software, board and hardware level. Attendees get some hands-on practice on Ultra Low Power MCU to illustrate what can be achieved by making use of energy saving techniques. MCU architecture is explained, energy aspects of various memory types plus some real-life use cases are presented.

**Class 5.5** 12.03.2026, 9:30 – 16:30**Embedded Software Testing – With Fundamental  
Skills and Artificial Intelligence***Dr. Stephan Grünfelder, Stephan Grünfelder*

After a review of proven, practical test methods applicable to all types of embedded SW, including testing in resource-constrained environments, data race detection, and real-time verification, we show which technique to apply in which stage of the SW development process. And we explore how AI-based techniques are entering the field of embedded testing, assisting with numerous testing tasks. In a live demo, participants will see where AI excels in testing – and explore the exciting frontier of what's becoming possible with current AI capabilities.

	1. IOT & CONNECTIVITY		2. EMBEDDED OS		3. SAFETY & SECURITY	
10:00-10:15	<b>Words of Welcome</b> Prof. Dr. Axel Sikora, Offenburg University					
10:15-10:45	<b>Conference Keynote: Learning from the Octopus: Nature's Blueprint for Intelligence Everywhere</b> Rich Simoncic, Microchip Technology					
	<b>1.1: Ambient IoT</b>  Ambient IoT Alliance		<b>1.4: WiFi and Long-Range</b>		<b>2.1: Long-Term Stability with Yocto</b> 	
11:00-11:30	<b>The Ambient IoT Alliance: Mission, Vision, and the Path to Pervasive Connectivity</b> Stephen Statler, Ambient IoT Alliance		<b>Wi-Fi HaLow The Future of Long-Range Connectivity is Here!</b> Dr. Easen Ho, Vantron Technology		<b>Linux Kernel Hardening With the Yocto Project</b> Michael Opendacker, Root Commit	
11:30-12:00	<b>Ambient IoT in Action</b> Simon Ford, Blecon Ltd		<b>Wi-Fi 8: A Deep Dive into IEEE802.11bn for Ultra-High Reliability</b> Joerg Koepp, Rohde & Schwarz		<b>Beyond the Release: Managing Long-Term Risk and Compliance in Embedded Linux with Yocto</b> Anna-Lena Marx, inovex	
12:00-12:30	<b>Security and Privacy for Ambient IoT: Challenges and Options</b> Preeti Ohri Khemani Infineon Technologies		<b>Long-range Low-power Communications: Advancements in LoRa, WM-Bus, mioty, and NB-IoT</b> Victor Royant, STMicroelectronics		<b>Linux Kernel Upgrades in Yocto: Strategy, Constraints, and Vendor Support</b> Enrico Bragante, Witekio	
12:30-12:45	Discussion/Q&A		Discussion/Q&A		Discussion/Q&A	
Lunch Break & Networking						
	<b>1.2: IoT Ecosystem Technologies 1</b>		<b>1.5: CAN Technologies</b> 		<b>2.2: Yocto Use Cases</b> 	
13:45-14:15	<b>Scaling Edge AI for the IoT Era: From Fragmented Devices to an Intelligent, Connected Edge</b> Iri Trashanski, Ceva		<b>CAN XL &amp; FD are Ready for the SDV</b> Dr. Arthur Mutter Robert Bosch		<b>TPM-Based Disk Encryption on Raspberry Pi with Yocto</b> Josef Holzmayr, Northern.tech Inc. (Mender.io)	
14:15-14:45	<b>Securing Device Credential Provisioning: Matter and the Wider IoT Ecosystem</b> Dr. Xin Qiu, Aurora Networks		<b>Tunneling and mapping of CAN-based communication via Ethernet and Bluetooth</b> Dr. Martin Merkel CAN in Automation (CiA)		<b>Maintaining ROS on Yocto: A Survival Guide for Embedded Open Source Integrators</b> Rob Woolley, Wind River	
14:45-15:15	<b>Zigbee 4.0: Connecting Devices Safely, with Low Power Efficiency Across Generations</b> Faisal Bhaiyat, Silicon Labs		<b>Embedded AI and CAN Networking</b> Holger Zeltwanger CAN in Automation (CiA)		<b>Modern Yocto Linux Best Practices: Evolving Beyond the Basics</b> Margarita Manterola Rivero, Igalia	
15:15-15:30	Discussion/Q&A		Discussion/Q&A		Discussion/Q&A	
Coffee Break & Networking						
	<b>1.3: IoT Ecosystem Technologies 2</b>		<b>1.6: CAN Safety &amp; Security</b> 		<b>2.3: RTOS Orchestration</b>	
16:00-16:30	<b>Hybrid IoT Connectivity Solutions for Smart Homes and Smart Factories</b> Andrés Muñoz, Microchip Technology		<b>Functional Safety in CAN XL</b> Robert Nawrath, DCD-SEMI		<b>Choosing the Right Software Foundation: Bare-Metal, RTOS, or Embedded Linux</b> Ed Langley, Witekio	
16:30-17:00	<b>Multiprotocol Connectivity in Smart Homes: Enhancing Interoperability and User Experience</b> Devanjan Sikdar, Silicon Labs		<b>Enhancing Functional Safety &amp; Security Aspects of CAN XL in Automotive Systems</b> Dr. Nikos Zervas, Computer Aided Software Technologies Inc. (CAST)		<b>Real-Time Meets Cloud: Orchestrating RTOS and Linux with Kubernetes</b> Andrei Kholodnyi, Wind River	
17:00-17:30	<b>Ambient IoT at µW Budgets: A 2026 Update Across 3GPP, IEEE 802.11, and Bluetooth LE</b> Stephen Statler, Infineon Technologies		<b>Overview of Emerging CAN Security Standards in the Context of CRA and IEC 62443</b> Christian Keydel, Embedded Systems Academy		<b>Beyond Cyclictest: a Unified Benchmark Framework for POSIX Compliant RTOS on ARM Processor</b> Lei Zhou, Linaro	
17:30-17:45	Discussion/Q&A		Discussion/Q&A		Discussion/Q&A	

**3. SAFETY & SECURITY**
**4. HARDWARE DESIGN**
**5. SOFTWARE & SYSTEMS ENGINEERING**
**6. EMBEDDED VISION**

Words of Welcome  
 Prof. Dr. Axel Sikora, Offenburg University

**Conference Keynote: Learning from the Octopus: Nature's Blueprint for Intelligence Everywhere**  
 Rich Simoncic, Microchip Technology

<b>3.4: Open Source for Safety &amp; Security 1</b>	<b>4.1: Chiplets in Automotive Applications</b> 	<b>5.1: Programming Languages: Rust</b>	<b>5.4: Software Architectures</b> 	<b>6.1: Concepts and Standards</b>
<b>Open Functional Safety: Safety-Qualified Lifecycle with Sphinx</b> Christopher Zimmer, innotec	<b>Chiplets: A Game-Changer for Advanced Automotive Computing</b> Dr. Ericles Sousa, Cadence Design Systems / UCle AWG	<b>From C to Rust: Modernizing Firmware Development for Resource-Constrained Embedded Devices</b> Jürgen Fitschen, SSV Software Systems	<b>From Embedded Systems to Embedded Intelligence: Architectural Patterns for Autonomous Industrial Operations</b> Afshin Asli, Synaptrix Technologies	<b>How to Run Smart-Phone AI Models on a Microcontroller in Real-time With MicroPython</b> Kwabena Agyeman, OpenMV
<b>Approaches on Assessing Safe Usage of Linux</b> Kate Stewart, Linux Foundation	<b>Enabling Chiplet-Based Solutions for Autonomous Driving Systems</b> Gil Golov, Socionext Europe	<b>Reliable Real-time with Rust Using the Example of Automation Technology</b> Marc Fischer, Universität Stuttgart	<b>Building a Safety-Certifiable Open Middleware for POSIX-Based Automotive Platforms</b> Philipp Ahmann, ETAS (BOSCH)	<b>Take Back Control of Your Cameras with libcamera</b> Laurent Pinchart, Ideas on Board
<b>Leveraging Open Source for IEC 62443-Compliant Embedded Systems</b> Dr. Florian Kauer, Linutronix	<b>High-level Modelling Methodology to Evaluate Automotive Chiplet Archetypes</b> Dr. Diksha Moolchandani, imec	<b>Understanding the Rust Borrow Checker</b> Leonardo Held, Toradex	<b>A Complete Open-Source, Functionally Safe Software Stack for the Software Defined Vehicle</b> Dr. Oliver Pajonk, Elektrobit Automotive	<b>From Rule-based to Fully Autonomous Robots: How to Scale Physical AI through Reasoning</b> Ahmed Sadek, Qualcomm
Discussion/Q&A	Discussion/Q&A	Discussion/Q&A	Discussion/Q&A	Discussion/Q&A

Lunch Break & Networking

<b>3.5: Open Source for Safety &amp; Security 2</b>	<b>4.2: Chiplets – Certification, Validation &amp; Test</b> 	<b>5.2: Programming Languages</b>	<b>5.5: Development Processes for SW-Defined Vehicles (SDV)</b>	<b>6.2: Hardware Acceleration</b>
<b>Open Source for Safety-Critical Systems: A Landscape Exploration</b> Philipp Ahmann, ETAS (BOSCH)	<b>Building Trust and Transparency Across the Chiplet Ecosystem: A Standardized Security Framework</b> Prof. Dr. Sylvain Guilley, Secure-IC	<b>Rust Guidelines and Standards – A State of the Feld Report</b> Alex Celeste, Perforce Software	<b>SDV Applications for Automotive ECUs: Achieving Cybersecurity and Functional Safety Compliance Through a Holistic Software Product Lifecycle Management</b> Dr. Ahmed Majeed Khan, SystemWeaver	<b>CPU and Co-Processor Paradigms for Edge AI Inference: Implications for NPU Design</b> Omar Lone, Züricher Hochschule für Angewandte Wissenschaften (ZHAW)
<b>Owning the Stack: Open-Source Device Management Without SaaS Lock-In</b> Julien Vermillard, Clunky Machines	<b>Analyzing Fault Propagation and Coverage in Chiplet-Based SoCs with Improved Colored Petri Nets</b> Ernesto Cristopher Villegas Castillo, Cadence Design Systems	<b>Architecture-Aware C/C++ to Rust Migrations</b> Dr. Daniel Simon, The Qt Company	<b>A Performance Comparison Study of Embedded Hypervisors for Software-Defined Vehicles Developed in Rust and C/C++: Focusing on ARM-based MCU SoCs</b> Dr. Sang-Bum Suh, Perseus Co.	<b>FPGA + GPU: A Hybrid Vision for Embedded AI</b> Dr. Tony Albrecht, hema electronic
<b>AI for Managing Embedded Linux Vulnerabilities: Too Good to Be True?</b> Dr. Julien Bernet, The Embedded Kit	<b>Wafer-Level Test Concept for the UCle Interface</b> Alexander Persicke, Racyics	<b>Fuzion – A Language Designed for Safety-Critical Embedded Systems</b> Dr. Fridtjof Siebert, Tokiwa Software	<b>From Open Source to Automotive-Grade: Distributing Eclipse S-CORE for Safety-Critical and Real-Time Embedded Systems</b> Lars Bauhofer, Qorix	<b>Adaptive Multispectral Imaging with Onboard AI Based on a Reconfigurable FPGA Architecture</b> Filip Novoselnik, Protostar Labs
Discussion/Q&A	Discussion/Q&A	Discussion/Q&A	Discussion/Q&A	Discussion/Q&A

Coffee Break & Networking

<b>3.6: Trusted Artificial Intelligence</b>	<b>4.3: MIPI Interfaces</b> 	<b>5.3: MISRA SW-Coding Guidelines</b> 	<b>5.6: Open Source Software</b>	<b>6.3: Pipelines</b> 
<b>Integrating Edge AI in Safety-Critical Embedded Systems – Safety Still Ensured?</b> Eranyan Ravanan, Hitex GmbH	<b>MIPI I3C Serial Bus: Latest Features and Market Applications</b> Michele Scariatella, MIPI Alliance	<b>MISRA – A Year in Review, and a Look Ahead</b> Andrew Banks, LDRA	<b>Understanding Open Source License Compliance in an OTA Situation</b> Josef Holzmayer, Northern.tech Inc. (Mender.io)	<b>Synchronized Vision Pipelines for Efficient Multi-Camera Perception</b> Florian Netter, Advanced Micro Devices (AMD)
<b>From Secure DFT to Lifecycle Security: Enabling SLM in Complex AI/HPC SoCs</b> Dr. Shahram Mossayebi, Crypto Quantique	<b>Turning Up the Volume: How SoundWire I3S Transforms Embedded Audio</b> Ettore Antonino Gilberti, SmartDV	<b>MISRA C:2023 &amp; MISRA C++:2023: So Close Yet So Different</b> Loïc Joly, SonarSource	<b>Open Source Hardware-in-the-Loop Testing</b> Detlef Vollmann, vollmann engineering	<b>Efficient Image Registration Methodology for Depth and RGB Camera</b> Sagar Dhattrak, elfin chips - an Arrow Company
<b>AI-Powered Intrusion Detection at the Edge: Hardware Anchors for Software Resilience</b> Prof. Dr. Sylvain Guilley, Secure-IC	<b>Wired for Intelligence: SWI3S The New Sensor Interface for Ambient AI</b> Manuela Heiss, Infineon Technologies	<b>High-Quality Code Meets Industry Standards: Linux and MISRA in Perspective</b> Prof. Dr. Roberto Bagnara, BUGSENG / University of Parma	<b>Free But Not Cheap: The Journey of Productizing Open Networking Software</b> Bruno Banelli, Sartura	<b>Power-Efficient AI at the Edge: Real-World Gains With Model Sparsity</b> Dean Leo, Microchip Technology
Discussion/Q&A	Discussion/Q&A	Discussion/Q&A	Discussion/Q&A	Discussion/Q&A

	1. IOT & CONNECTIVITY		2. EMBEDDED OS		3. SAFETY & SECURITY	
	<b>1.7: Ethernet Time-Sensitive Networking (TSN)</b>	<b>1.10: Cellular – Emerging Technologies</b>	<b>2.4: Zephyr – Best Practice</b>		<b>3.7: Reliable Architectures</b>	
10:00-10:30	<b>Maintaining Time Synchronization in High Network Traffic Applications</b> Schuyler Patton, Texas Instruments	<b>Enhancing Road User Safety in Connected Vehicles: Real-World 5G C-V2X Applications</b> Andrei Kholodnyi, Wind River	<b>Zephyr: 10 Years After Launch</b> Kate Stewart, Linux Foundation		<b>What is the Future of Using Standard Complex Semiconductors in Safety Applications?</b> Alessandro Bastoni, STMicroelectronics	
10:30-11:00	<b>Harnessing Linux Timekeeping for Multi-Domain Precision Time Protocol in Time-Sensitive Networking</b> Weifeng Voon, Intel	<b>Sky-High RAN: Bridging Terrestrial to Satellite in 5G/6G with FPGAs</b> Dr. Hossam Fattah, Lattice Semiconductor	<b>How to Migrate from FreeRTOS to Zephyr RTOS</b> Jacob Beningo, Beningo Embedded Group		<b>Most Automotive MPU Strategies Have Hidden Safety Flaws, Is Yours One of Them?</b> Kevin Brand, Synopsys	
11:00-11:30	<b>Hard-Earned Wisdom from TSN Interop Events: Lessons You Can't Afford to Miss</b> Ionel Ghita, Keysight Technologies	<b>Voice Over NB-IoT NTN – Is it Viable?</b> Richard Carter, Communications Consultants WorldWide	<b>Practical Zephyr: Boosting Your Embedded Workflow</b> Benjamin Cabé, The Zephyr Project		<b>The Challenge of Sharing: Building Safe Mixed-Criticality Systems</b> Ofra Bechor, Green Hills Software	
11:30-11:45	Discussion/Q&A	Discussion/Q&A	Discussion/Q&A		Discussion/Q&A	
Lunch Break & Networking						
	<b>1.8: Single-Pair Ethernet</b>	<b>1.11: Cellular – 5G</b>	<b>2.5: Zephyr in Safety-Critical Applications</b>		<b>3.8: Reliable Code / Safe Rust</b>	
12:45-13:15	<b>Extending Ethernet to the Industrial Edge: Practical Insights into 10BASE-T1L and PoDL Deployment</b> Nina Lai, Netio Technologies Co.	<b>Securing the Next Wave of Connectivity: 5G Cybersecurity Challenges and Solutions for Embedded IoT Systems</b> Simon Mullenger, Telit Cinterion	<b>Zephyr's Roadmap to a Pre-Certified Kernel for Safety-Critical Systems</b> Dr. Tobias Kästner, inovex		<b>How To Use Formal Methods To Detect Runtime Faults in Mixed C, C++ &amp; Rust Codebases</b> Steve Barriault, TrustInSoft	
13:15-13:45	<b>Increasing Fault Tolerance of 10BASE-T1S Multidrop Networks with PLCA Coordinator Redundancy</b> Arndt Schübel, onsemi	<b>MicroTCA Next Gen: A New Backbone for High-Performance Embedded Systems</b> Brandon Lewis, Samtec	<b>Turning the Ignition on Safety: Zephyr RTOS in Automotive Compliance</b> Parthiban Nallathambi, Linumiz		<b>Addressing Functional Safety with Rust</b> Jill Britton, Perforce	
13:45-14:15	<b>Classic Connection Technology Meets Modern Data Transmission – PCB Terminal Blocks Enable Single Pair Ethernet (SPE)</b> Andy Schäfer, Phoenix Contact	<b>Open, Agile, Intelligent: The Future of 5G with AI and ORAN</b> Dr. Hossam Fattah, Lattice Semiconductor	<b>Industrializing Zephyr for Safety-Critical Products: A Four-Pillar CI Playbook</b> Prof. Dr. Roberto Bagnara, BUGSENG / University of Parma		<b>Rust on the Road: Navigating Challenges and Opportunities in Automotive</b> Sjoerd van der Zwaan, Solid Sands	
14:15-14:30	Discussion/Q&A	Discussion/Q&A	Discussion/Q&A		Discussion/Q&A	
Coffee Break & Networking						
	<b>1.9: Applying Ethernet Technologies</b>	<b>1.12: Cellular – eSIM</b>	<b>2.6: Zephyr Use Cases</b>		<b>3.9: Reliability Testing</b>	
15:00-15:30	<b>Simplifying Multi-Protocol Industrial Ethernet: One Design, Every Protocol</b> Thomas Mauer, Texas Instruments Deutschland	<b>How SGP.32 eSIM Accelerates Secure Supply Chain Digitalization</b> Cyril Proye, Thales	<b>Zephyr Squared: Zephyr and Linux 'Side by Side' on the Same Device</b> Hugh Breslin, Microchip Technology		<b>Safety and Security by Design Through Formal Methods</b> Mark Hermeling, AdaCore	
15:30-16:00	<b>Debugging a System of Microcontrollers over Ethernet</b> Dr. Albrecht Mayer, Infineon Technologies	<b>Realising the Transformative Potential of eSIM for the IoT</b> Stéphane Jacquelin, IDEMIA	<b>The RTOS Puzzle: How Far Can We Go in Vulnerability Management? A Zephyr Case Study</b> Pierre Gal, The Embedded Kit		<b>Sound Static Application Security Testing</b> Dr. Daniel Kästner, AbsInt Angewandte Informatik	
16:00-16:30	<b>Leveraging High-speed Ethernet for Scalable Audio in Automotive Zonal Control Systems</b> Emanuele Castronuovo, STMicroelectronics	<b>How eSIM is Evolving into a Multi-Application Secure Platform</b> Gil Bernabeu, GlobalPlatform	<b>How Zephyr Delivers Low Power</b> Dr. Ayoub Bourjilat, AC6		<b>Hyper Coverage with Integration Testing: How Can I Get Half of My Test Cases for Free?</b> Dr. Alexander Weiss, Accemic Technologies	
16:30-16:45	Discussion/Q&A	Discussion/Q&A	Discussion/Q&A		Discussion/Q&A	

4. HARDWARE DESIGN	5. SOFTWARE & SYSTEMS ENGINEERING	6. EMBEDDED VISION	7. EDGE AI	8. USE CASES FOR EMBEDDED
<b>4.4: System on Chip Design Process</b>	<b>5.7: Testing Embedded Software</b>	<b>6.4: Emerging Embedded Vision &amp; Audio Technologies</b>	<b>7.1: Lightweight Embedded AI</b>	<b>8.1: Medical Applications</b>
<b>Bridging the Virtual and Physical Divide: A Comparative Methodology for Validating Complex SoCs</b> Prashant Yadav, The Judge Group	<b>Unit Testing for Embedded Development: From Real Silicon to Emulated Environments</b> Ilia Motorny, JetBrains	<b>Extreme Low-bit Quantization for Real-world Edge AI</b> Daniel Chang, ENERZAI	<b>Tiny Foundation Models: Exploring Scalable Pretrained Architectures for Embedded AI</b> Nitish Kumar, The Judge Group	<b>Sustaining Medical Devices: The Long-Term Support Imperative</b> Dr. Julian Bernet, Witekio
<b>Evaluating Tiled Convolution Designs on SoC-FPGA with Unified HW/SW Performance Metrics</b> Prof. Dr. Guy Bois, Polytechnique Montreal	<b>Agile Testing for Microcontroller Projects – What are Realistic Objectives?</b> Daniel Penning, embeff	<b>Unlock Real-Time Visual Intelligence with Generative AI at the Edge</b> Kevin Patel, NVIDIA	<b>Lightweight and Secure MCP for Embedded AI: Bringing Agent Protocols to the Edge</b> Jürgen Belz, PROMETO	<b>Confronting the Connectivity Challenge in Endoscopic and Robotic Surgeries</b> Jonathan Regalado-Hawkey, Valens Semiconductor
<b>Design of Domain Specific Accelerators with High-Level Synthesis</b> Prof. Russell Klein, Siemens EDA	<b>Did We Test the Right Things? Prevent Production Defects with Test Gap Analysis</b> Jonas Bogenberger, CQSE	<b>From Foundation to Factory: Adapting Foundational Vision Encoders to Custom OCR at the Edge</b> Alex Avery, D3 Embedded	<b>Generate Plain C/C++/CUDA Code from TensorFlow and PyTorch Models Using MLIR</b> Christoph Stockhammer, The MathWorks	<b>Design Review of Embedded Medical Sensor &amp; Camera Platform with Emphasis on Medical EMC Solutions</b> Ozan Günaydin, Brainlab/Snke OS
Discussion/Q&A	Discussion/Q&A	Discussion/Q&A	Discussion/Q&A	Discussion/Q&A
Lunch Break & Networking				
<b>4.5: System Hardware – Design Examples</b>	<b>5.8: Trustable Embedded Software</b>	<b>6.5: EV Use Cases</b>	<b>7.2: Neuromorphic Computing</b>	<b>8.2: Predictive Maintenance Applications</b>
<b>Deterministic Software Co-Design of RL-Tuned iLQR Controllers on Embedded SoC Systems</b> Marco Torelli, TXT e-tech	<b>Eclipse Trustable Software Framework: A New Industry Standard for Embedded Systems</b> John Ellis, Codethink	<b>Extending HDR Capabilities in Smart Vision Systems via Multi-Exposure Fusion and Adaptive Tone Mapping</b> Dr. Alex Lopich, Altera	<b>Neuromorphic Deployments Made Easy: from Datasets to Applications</b> Dr. Petrut Antoniu Bogdan, Innatera Nanosystems	<b>Modernizing Railway Brake Diagnostics: A Raspberry Pi DAQ Approach</b> Prof. Dr. Georgi Nikolov, Darmstadt University of Applied Sciences
<b>Designing Smart Displays with STM32 MCUs: Usecases from Industrial, Automotive, and Medical Applications</b> Rhett Evans, Anders Electronics	<b>AI-Generated Code for Critical Systems: Can We Trust It?</b> Miroslaw Zielinski, Parasoft	<b>Enhancing Industrial Visual Inspection with Expert-guided, Feedback-driven AI</b> Lena Heidemann, Fraunhofer IKS	<b>Going Beyond the von Neumann Wall: In-Memory and Neuromorphic Computing for Efficient Embedded AI</b> Sebastian Karl, Fraunhofer IIS, Fraunhofer Institut für Integrierte Schaltungen	<b>Motor Predictive Maintenance Using Edge AI</b> Dr. Han Zhang, Texas Instruments
<b>Benefits of Embedded Mixed Signal IC Solutions for Type-C Rapid Battery Charger Applications</b> Dr. Robert Vartanian, Infineon Technologies	<b>Safely and Securely Combining Trusted Rust Code with Untrusted Software</b> Andre Schmitz, Green Hills Software	<b>Isolated Camera Serial Interface Integration with GMSL for High-Reliability Imaging Systems</b> Prasanthi Yerra, Analog Devices	<b>New Semiconductor Platform for Neuromorphic Computing and Gen 3.0 In-Memory Edge AI Applications - The Embedded TiF-Memristor-Xbar</b> Prof. Dr. Heidemarie Krüger, TECHiFAB	<b>Vibration Monitoring: Integrating Precision Sensing with Edge AI Processing</b> Dr. Lisa Trollo, STMicroelectronics
Discussion/Q&A	Discussion/Q&A	Discussion/Q&A	Discussion/Q&A	Discussion/Q&A
Coffee Break & Networking				
<b>4.6: Architectural Design</b>	<b>5.9: Formal Verification</b>	<b>6.6: Radar and Artificial Intelligence</b>	<b>7.3: Qualification and Validation</b>	<b>8.3: Mobility Applications</b>
<b>Minimizing Power in Clock Domain Crossing: Architectural Innovations for SoC Design</b> Aradhana Kumari, STMicroelectronics	<b>Formal Verification in Practice: Experiences from Embedded Software Projects</b> Markus Krahl, Munich University of Applied Sciences HM	<b>Applying Artificial Intelligence in Radar Sensing Applications</b> Kottyn Quintanilla, Texas Instruments	<b>Qualification of AI/ML Systems and Interfacing Devices</b> Steve DiCamillo, LDRA	<b>Bringing Native Maps and Navigation to Resource-Constrained MCUs</b> Sumitabh Ghosh, Qt Group
<b>MIPI A-PHY as an Enabler for Remote Multi-Head “Smart Camera” Architecture</b> Jonathan Regalado-Hawkey, Valens Semiconductor	<b>Usage of Formal Methods in Embedded Software Development to Automate Test Case Generation Based on Model Coverage Gaps</b> Vincent Rossignol, Ansys, part of Synopsys	<b>Radar Development Essentials: Overcoming Complexity with the Right Tools</b> Dr. Dave Bethge, NXP Semiconductors Germany	<b>Implementing ISO/PAS 8800: 2024 to Assure Safety and Enable Deployment of AI in Embedded Systems</b> Ricardo Camacho, Parasoft	<b>Enhancing Steering Wheel Safety Through AI-Based Signal Correction</b> Jasmin Frick, invenio
<b>AI-Driven NoC Topology Optimization for Large-Scale SoC Designs</b> André Bonnardot, Arteris	<b>Making Software Formal Verification Methods A Viable Technique In An Industrial Setting</b> Steve Barriault, TrustInSoft	<b>Imaging Radars for Physical AI</b> Dr. Gor Hakobyan, Waveye	<b>From Cloud to Edge: Digital Twin Frameworks for Real-Time Autonomous System Validation</b> Nitish Kumar, The Judge Group	<b>Radar and Lidar Fusion for Enhanced Perception in Urban Air Mobility</b> Marco Roggero, The MathWorks
Discussion/Q&A	Discussion/Q&A	Discussion/Q&A	Discussion/Q&A	Discussion/Q&A

	1. IOT & CONNECTIVITY	2. EMBEDDED OS	3. SAFETY & SECURITY	4. HARDWARE DESIGN
	<b>1.13: Bluetooth –  Bluetooth™ Best Practices</b>	<b>2.7: Container Use Cases</b>	<b>3.10: Ensuring Resilient Embedded Systems</b>	<b>4.7: Hardware Design &amp; Production Process  ← Wir verbinden</b>
09:30-10:00	<b>Data-Driven Bluetooth LE Development: Measuring What Matters for Connection Stability and Power Efficiency</b> Gillian Minnehan, Nordic Semiconductor	<b>Managing Container Updates – Challenges and Solutions</b> André Detsch, Foundries.io	<b>100 Million Inputs or it Did Not Happen: Fuzzing Full Embedded Software Via Rehosting</b> Tobias Scharnowski, CISPA Helmholtz Center for Information Security	<b>The Challenge of Sharing Structured Knowledge with GenAI Tools</b> Jürgen Mayer-Zintel, Infineon Technologies
10:00-10:30	<b>Precision Distance Measurement with Bluetooth Channel Sounding - The Technical Case for Multi Antenna Support</b> Jonathan Kaye, Ezurio	<b>Commodization of Distro Building: Why Bootable Containers Will Transform Embedded Linux Development</b> Leonardo Held, Toradex	<b>From Firmware to Keys: Reverse Engineering Cryptography in Embedded Devices</b> Dr. Nils Albartus, Emproof	<b>Good Documentation Practices Meet Modern, Development and Design Needs</b> Dr. Marco Häuser, Marco Häuser Design   MHD
10:30-11:00	<b>Building Distributed Beacon Networks with Bluetooth</b> Donatien Garnier, Blecon	<b>From Regret to Reproducibility: Why Embedded Workflows Belong in Containers</b> Felipe Torrezan, IAR	<b>Inherent Trust: How Hardware Identity can Secure the Global Supply Chain</b> Dominic Rizzo, ZeroRISC	<b>Approach to Optimize Quality, Cost and Delivery for PCBs</b> Georg Thämer, Festo SE
11:00-11:15	Discussion/Q&A	Discussion/Q&A	Discussion/Q&A	Discussion/Q&A
Coffee Break & Networking				
	<b>1.14: Bluetooth –  Bluetooth™ Emerging Technologies</b>	<b>2.8: Beyond Virtualization</b>	<b>3.11: DevSecOps for Safe &amp; Secure Systems</b>	<b>4.8: Hardware Design Examples</b>
11:45-12:15	<b>Standardizing Ultra-low Latency HID with Bluetooth Technology</b> Alfredo Perez, Bluetooth SIG	<b>Reevaluating the Role of Hypervisors in Safe and Secure Software Partitioning</b> Marcus Nissemark, Green Hills Software	<b>Secure By Default: DevSecOps Workflows for CRA-ready Embedded Systems</b> Dr. Marc Thomas, IAR	<b>PCB-Design of High-Speed Boards</b> Prof. Rainer Thüringer, TH-Mittelhessen
12:15-12:45	<b>Enhancing the Responsiveness of Bluetooth Gaming Controllers with HID ISO</b> Jan Slupski, Telink Semiconductor	<b>Containers for Embedded Linux; The Next Chapter</b> Drew Moseley, Toradex	<b>Agent-Driven DevSecOps: Transforming Embedded Software Development</b> Rainer Poisel, honeytreeLabs Cooperation	<b>DC to AC Conversion With DC to DC Buck Converters for PDLC Displays</b> Andrew Kutzler, Texas Instruments
12:45-13:15	<b>An Overview of Bluetooth High Data Throughput</b> Damon Barnes, Bluetooth SIG	<b>When Docker Doesn't: What Embedded Engineers Need to Know</b> Joe Schneider, Dojo Five	<b>Next Level DEVSECOPS for a Functional Safety Software Development Process</b> Jeffrey Fortin, Vector Informatik	<b>From Earth to Orbit: The Essential Role of Antennas in NTN-IoT</b> Carmen Redondo, Kyocera AVX
13:15-13:30	Discussion/Q&A	Discussion/Q&A	Discussion/Q&A	Discussion/Q&A
Lunch Break & Networking				
	<b>1.15: Bluetooth in  Bluetooth™ Automotive Applications</b>	<b>2.9: Real-Time Virtualization</b>	<b>3.12: Trustworthy  CHERI Systems with CHERI &amp; RISC-V</b>	<b>4.9: Power Supply Design</b>
14:30-15:00	<b>Modular Architecture for Enhanced Vehicle Access with Bluetooth Channel Sounding</b> Martin Cuvelier, NXP Semiconductors	<b>Embedded Virtualization on Arm v8-R: When You Need It, and When You Don't</b> Dr. Carmelo Loiacono, Green Hills Software	<b>Building Safe and Secure Systems with RISC-V</b> Gerard Vink, TASKING	<b>Comparison of Wireless Power Transfer Methods, Simulation and Analysis of a Standard Resonant Converter Design</b> Dr. Willy Stephen Tounsi Fokui, Teleconnect
15:00-15:30	<b>Seamless Handover of Bluetooth LE Connections for Enhanced User Experience</b> Christin Lee, Texas Instruments	<b>An Open Hypervisor for Automotive Zonal Controllers</b> José Martins, OSYX Technologies	<b>CHERI Standardization For All RISC-V Processors From Tiny to Huge</b> Tariq Kurd, Codasip	<b>Comparing Solar Cells and Power Management Circuits Used for Indoor Low Power Wireless Embedded Systems</b> Prof. Dr. Marcel Meli, Applied Science University of Winterthur
15:30-16:00	<b>Secure Localization with Bluetooth Channel Sounding for Localization and Smart Keys in Automotive Systems</b> Sindhur Sondur, OpenSynergy	<b>Beyond Containers and VMs: Are Unikernels the Next Stage in Real-Time Virtualization?</b> Matthias Richter, Universität Stuttgart	<b>Industrializing CHERI on RISC-V: VxWorks and Hypervisor Support for Safety-Critical Edge Systems</b> Dmitriy Yeliseyev, Wind River	<b>Reliable Power Supplies: Overvoltage and Avalanche Energy in Mosfets</b> Prof. Markus Rehm, IBR Ingenieurbüro Rehm
16:00-16:15	Discussion/Q&A	Discussion/Q&A	Discussion/Q&A	Discussion/Q&A

4. HARDWARE DESIGN	5. SOFTWARE & SYSTEMS ENGINEERING		7. EDGE AI	8. USE CASES FOR EMBEDDED
<b>4.10: RISC-V® RISC-V Ecosystem</b>	<b>5.10: DevOps &amp; CI/CD Pipeline</b>	<b>5.13: Digital Twin</b>	<b>7.4: Execution</b>	<b>8.4: Development Processes</b>
<b>The Growing Software Ecosystem for RISC-V</b> Richard York, SiFive	<b>Platform Integrated AI Reduces The Cognitive Load of Onboarding to Embedded DevOps</b> Collen Lake, GitLab	<b>Security First: Why Digital Twins Need a Trusted Foundation</b> Sebastian Rohr, umbrella.associates	<b>A Review, a Proposal and an Extrapolation on the Theme of Edge AI Execution Frameworks</b> Prof. Hans Dermot Doran, Zürcher Hochschule für Angewandte Wissenschaften (ZHAW)	<b>Informed Systems Engineering Decision-making Through SysML v2 Modelling with Architecture Simulation</b> Dr. Bernhard Kaiser, Ansys Germany
<b>Scalable Benchmarking and Profile-Based Alignment for RISC-V Ecosystems</b> Angel Berrio, Quintauris	<b>Using CI/CD for Grass Roots Software Quality Improvements</b> Mark Hermeling, AdaCore	<b>Lightweight Digital Twins and Co-Simulation for Physical AI</b> Dr. Pablo Oliveira Antonino, Fraunhofer IESE	<b>Deploying Energy-Efficient Machine Learning at the Edge: A Practical Approach</b> David Fosca Gamarra, Texas Instruments	<b>WinLightNet: A Self-Distillation Technique for Time Series Classifications on Constrained Devices</b> Ghaia Belaakaria, Schneider Electric
<b>Toward a Holistic Compute Platform for Mixed-Criticality RISC-V Platforms</b> Dr. Sandro Pinto, University of Minho	<b>DevOps for Systems Engineering in Software-defined Vehicles</b> Dr. Frank Schreiner, AUMOVIO Engineering Solutions	<b>Virtual Prototypes for Embedded Systems – Transforming Product Development</b> Christopher Schwager, CarByte Engineering	<b>Running Transformer Models Efficiently on Edge Devices with Static AI Engines</b> Sauryadeep Pal, Synaptics	<b>Pipeline-first Co-design for Embedded Time-series Classification: Post-layout Cost-aware Joint Optimization of Feature Extraction and Inference</b> Dr. Lilli Frison, Hahn-Schickard-Gesellschaft für angewandte Forschung e.V.
Discussion/Q&A	Discussion/Q&A	Discussion/Q&A	Discussion/Q&A	Discussion/Q&A
Coffee Break & Networking				
<b>4.11: RISC-V® RISC-V Applications</b>	<b>5.11: Workflows and Tools</b>	<b>5.14: SW Debugging and Tracing</b>	<b>7.5: From Lab to Field</b>	<b>8.5: Security Applications 1</b>
<b>Extending RISC-V into VLIW/SIMD Architectures for Application-Specific Workloads</b> Gert Goossens, Synopsys	<b>Rapid Prototyping of Autonomous Driving Algorithms on Embedded Platforms Using Docker and MATLAB</b> Benedikt Schlereth-Groh, Technische Hochschule Nürnberg Georg Simon Ohm	<b>Unified Tracing for Zynq UltraScale+ CPU and Programmable Logic in One View</b> Albert Schulz, Accemic Technologies	<b>From Lab to Field: Operating AI Models Across Thousands of Edge Devices</b> Carl Moberg, Avassa	<b>Securing Defence Software: From Threat Modelling to Long-Term Maintenance</b> Dr. Julian Bernet, Witekio
<b>Utilizing the RISC-V Architecture to Accelerate Real-Time Applications</b> Sean Murphy, MIPS Tech	<b>Modern IDE Workflows for Kernel Linux Module Debugging</b> Matheus Castello, Toradex	<b>Debugging the Invisible: Observability Techniques for Embedded RTOS Systems</b> Dr. Carmelo Loiacono, Green Hills Software	<b>Faster to Efficient and Reliable Edge AI Solutions with Automated MLOps</b> Dr. Axel Plinge, Fraunhofer IIS	<b>No Safety Without Security: Tool-Supported Co-Engineering for Automotive Systems</b> Roman Trentinaglia, Fraunhofer IEM
<b>Real-Time Signal Processing and AI on a RISC-V CGRA</b> Prof. Dr. Christian Siemers, Ubitium	<b>Platform, Not Product: Modernizing RCP with Theia/VSCoDe and a Broader Tech Ecosystem</b> Enrico Bragante, Infineon Technologies Italia	<b>Accelerating SDV Development with Cloud Debugging and Profiling on Automotive Platforms</b> Vittorio Serra, Lauterbach	<b>Agentic Generative AI on Embedded Devices</b> Michaël Uyttersprot, Avnet Silica	<b>Importance of IEC 62443 for Upcoming Regulations</b> Michelle Michael, TÜVIT
Discussion/Q&A	Discussion/Q&A	Discussion/Q&A	Discussion/Q&A	Discussion/Q&A
Lunch Break & Networking				
<b>4.12: Open-Source SoC Hardware</b>	<b>5.12: Technical Debt and Legacy</b>	<b>5.15: Generating Flexible &amp; Efficient Code</b>	<b>7.6: Use Cases</b> 	<b>8.6: Security Applications 2</b>
<b>Taping-out Open-Source Hardware and the Reproducibility Gap</b> Dr. Augusto Hoppe, Fraunhofer IIS	<b>The Breeding and Rearing of Technical Debt</b> Ingo Nickles, Vector Informatik	<b>Honey, I Blew Up the Code. Binary Size Reduction in Practice</b> Dr. Andreas Wilhelm, CQSE	<b>Using Industry-standard AI Techniques to Solve Real-world Display Problems at the Edge</b> Dave Gillespie, Synaptics	<b>Automated Identity Management for Embedded Components</b> Florian Handke, Campus Schwarzwald
<b>Open-Source Silicon: Driving Innovation, Trust, and Security in Embedded Systems</b> Dominic Rizzo, ZeroRISC	<b>Avoiding New ECU Development: Unlocking Hidden Potential in Legacy Systems</b> Dominik Jürgens, tensor embedded	<b>Web Engines for Embedded Devices: An Introduction to WPE WebKit</b> Mario Sanchez-Prada, Igalia	<b>Optimizing Neural Network Models for Low-Power Edge Hardware in Speech Processing Applications</b> Osman Erman Okman, Analog Devices (ADI)	<b>QSNP: The European Initiative for the Development of Quantum-Safe Networks</b> Iñaki Baretтини, ICFO
<b>Custom Open-Source FPGAs are Here</b> Prof. Dirk Koch, Universität Heidelberg	<b>Keep it 'clean': Practical Strategies for Reducing Build-System and Host Tech Debt</b> Joe Schneider, Dojo Five	<b>WebAssembly in Safety-Critical Embedded Systems: A Runtime for the Heterogeneous Future</b> Dan Milea, Wind River	<b>Lessons Learned Designing an Edge AI ASIC for Audio Applications</b> Matteo Vit, Starware Design	<b>From Cloud to Car: Edge AI in Next-Generation Automotive Cybersecurity</b> Gregor Knappik, VicOne
Discussion/Q&A	Discussion/Q&A	Discussion/Q&A	Discussion/Q&A	Discussion/Q&A



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